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LSI/VLSI ION IMPLANTED PLANAR GaAs IC PROCESSING

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The scope of this program was two-fold: (1) to complete and stabilize the development of a planar fabrication process for high speed digital integrated circuits on 3-inch GaAs wafers, and (2) to utilize gate arrays up to the 1K equivalent gate level as the demonstration circuits for this process development.

In addition to optimizing equipment and handling techniques for 3-inch GaAs wafers, the process development task concentrated on test chip characterization, threshold voltage uniformity control, and materials evaluation. Piezoelectrically generated device non-uniformities were a primary consideration during this time.

The gate array development involved two mask sets. The first was used to establish process and design criteria for gate arrays, as well as to fabricate a 5 x 5 multiplier. The second mask set was an extension of the previous work, and was used to fabricate gate arrays of the 1K equivalent gate complexity. The Mayo Foundation provided the expertise for auto-routing and personalization techniques.

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1.0 INTRODUCTION

Programs to develop GaAs ICs for such DoD applications as electronic warfare, secure communications and ballistic missile defense have been supported by several DoD agencies. These programs involve demonstration of circuits as complex as a 16-bit GaAs microprocessor. In addition, possible use of GaAs ICs in programs such as the Advanced Onboard Signal Processor (AOSP) is of strong interest because of the considerable radiation hardness of GaAs ICs. In order for these potential applications of GaAs ICs to progress beyond the feasibility demonstration stage, it has been essential to carry out further process development activities, directed towards processing improvements and a significant increase in the yield of complex GaAs ICs. The main objective of this program, therefore, was to complete and stabilize the development of a planar fabrication process for high speed digital integrated circuits on 3 in. diameter GaAs wafers. The demonstration vehicles for this process development were gate arrays up to the 1K gate level complexity. Additional tasks include an effort on mask programmable logic arrays related to ERADCOM needs, and a task to fabricate wafers for contractors to the DARPA Information Processing Technology office.

In this final report, the results from a number of specific tasks will be discussed. Of primary interest are the results from the two gate array mask sets which were utilized on the program. The first mask set, designated AR7, provided an opportunity to evaluate 3 in. GaAs wafer processing for large area circuits, as well as to develop the necessary design and modelling tools necessary for gate array development. The second mask set, designated AR8, was an extension of AR7, and raised the complexity of the gate array circuits to the 1K equivalent gate level. For the AR8 mask set, the Mayo Foundation provided the necessary personalization routines for implementation of the 8 × 8 multiplier; the demonstration circuit for this particular mask set. The personalization for the 5 × 5 multiplier, the demonstration circuit for the AR7 mask set was done by hand and provided the necessary input for the AR8 work. Although the personalization was done by hand, it utilized standard cell configurations, and the same routing channels as the automatic routing program.

In addition to the gate array work, considerable progress was made in the development and stabilization of the 3 in. wafer GaAs process. In conjunction with the SRAM development work being performed under Contract No. MDA703-83-C-0067, an extensive rework of the process quipment was undertaken. The main areas involved were photolithography, dielectric deposition and dry etching. This process dvelopment work has since become a standard for all 3 in. GaAs wafer processing at Rockwell.

2.0 PROCESS DEVELOPMENT

Prior to the start of this program, the majority of the 3 in. wafers processed had been ultra-low power RAM circuits and, as such, had been fabricated with several nonstandard steps such as low threshold voltage, proton isolation and cermet resistors. The first gate array mask set, designated AR7, has provided an opportunity to evaluate "standard" 3 in. GaAs wafer processing. During the course of the wafer fabrication, several processing details surfaced which required further investigation and evaluation. Of primary importance was wafer handling techniques to reduce breakage, and alignment mark corrections to improve exposure yield. Once these preliminary details were resolved, the process development activities concentrated on test structure yield studies and threshold voltage uniformity.

2.1 Process Techniques for Three Inch Wafers

One of the initial concerns regarding large diameter GaAs wafers was breakage, both by laboratory personnel, and by the various pieces of processing equipment. Because of the extensive handling by laboratory personnel, a certain amount of breakage is inevitable. However, the breakage due to the processing equipment can be minimized through careful equipment selection and fixturing design. An example is the low pressure chemical vapor deposition (LPCVD) system used for deposition of first level SiO_2. Figure 2.1-1 shows the wafer holders used in the system; the one on the left represents the initial design. The three tabs used to hold the wafer in place were found to induce localized stress and chipping and, as a result, several wafers were broken. The redesigned holder is shown on the right in Fig. 2.1-1 and was found to be much more satisfactory in reducing wafer breakage. In addition to the LPCVD system, other pieces of processing equipment, such as spinners and anneal furnaces, were modified to eliminate any potential breakage problems. It has taken several wafer runs through all the processing equipment in order to identify and correct breakage due to equipment fixturing. It should be noted that wafer breakage in the 10X wafer stepper was very minimal and, as such, demonstrated the feasibil-

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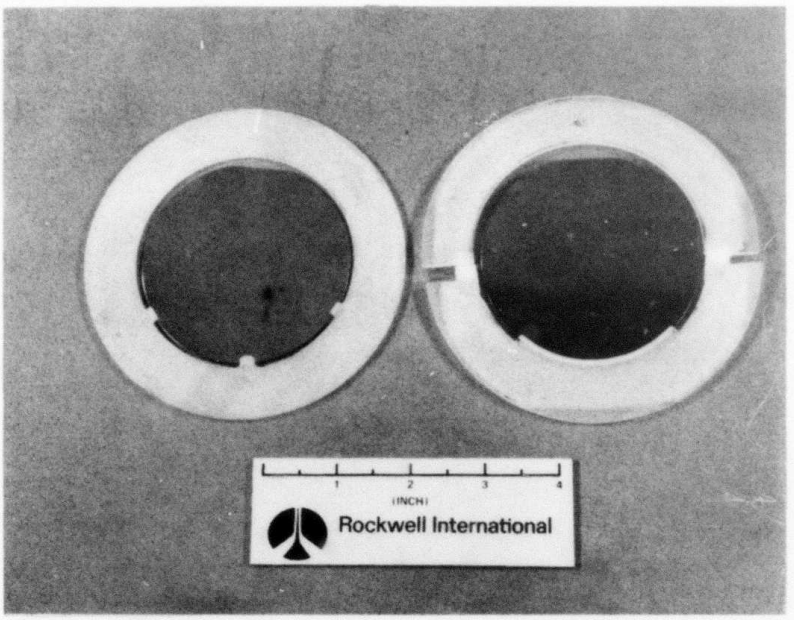

Fig. 2.1-1 Wafer fixtures for CVD system.

ity of using cassette-to-cassette wafer handling with large GaAs wafers. Edge beveling was used on all lot starts in order to reduce breakage by laboratory personnel. As Fig. 2.1-2 shows, tweezer chipping of the edge was initially a common problem and was reduced through use of the beveling process. Examples of beveled and nonbeveled wafer edges are shown in Fig. 2.1-3.

Techniques for optimization of lithography alignment marks were also improved in an effort to minimize the number of unexposed fields. It is imperative to have uniform, high contrast marks for the 10X wafer stepper, since alignment, focus and leveling are all dependent on the quality of the alignment signals. The various contrast mechanisms which can be used with the wafer stepper are illustrated in Fig. 2.1-4. Surface reflectivity, which is used for first level processing, and scattering, which is used for second level processing, are the two mechanisms used in the current 3 inch process. The thickness and uniformity of the various films deposited on top of the alignment marks is also crucial in obtaining good lithography yield and quality. As shown in

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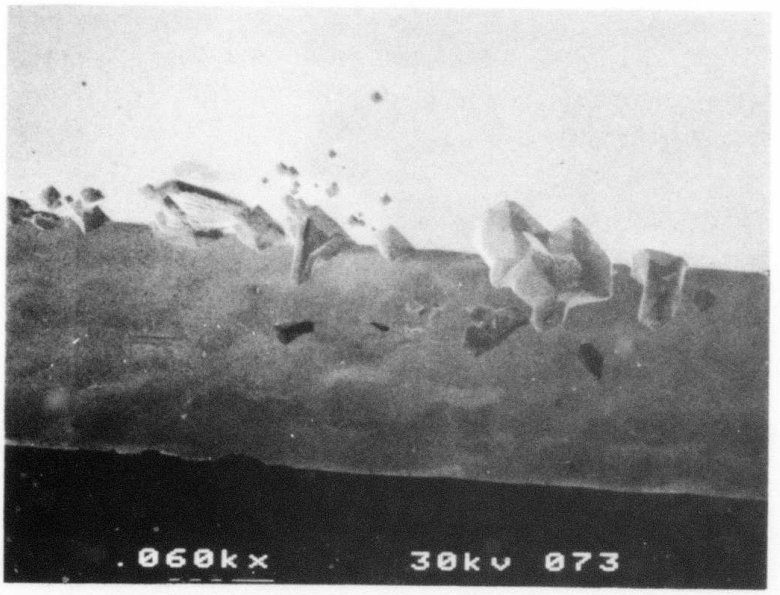


Fig. 2.1-2 Handling damages on unbeveled edge.

Fig. 2.1-5, intereference effects can degrade the reflected alignment signal to an almost undetectable level, depending on the thickness of the particular film.

As more lithography experience was gained, various pieces of equipment had to be modified in order to accommodate the reflectivity limits. For example, the existing spinners were precisely calibrated and the controls modified in order to maintain repeatable spin speeds. A new spin/bake system was brought on-line to further improve the reproducibility and uniformity of the resist films. The low pressure CVD system, as discussed previously, was modified to primarily reduce wafer breakage. However, the new holders degraded the oxide uniformity and, as a result, further modifications were necessary to help ease the resultant lithography problems. In spite of the shortcomings of the various pieces of processing equipment, the yield of properly exposed fields per wafer has increased to over 95%, up from the initial 70-90% when 3 in. wafer processing began.

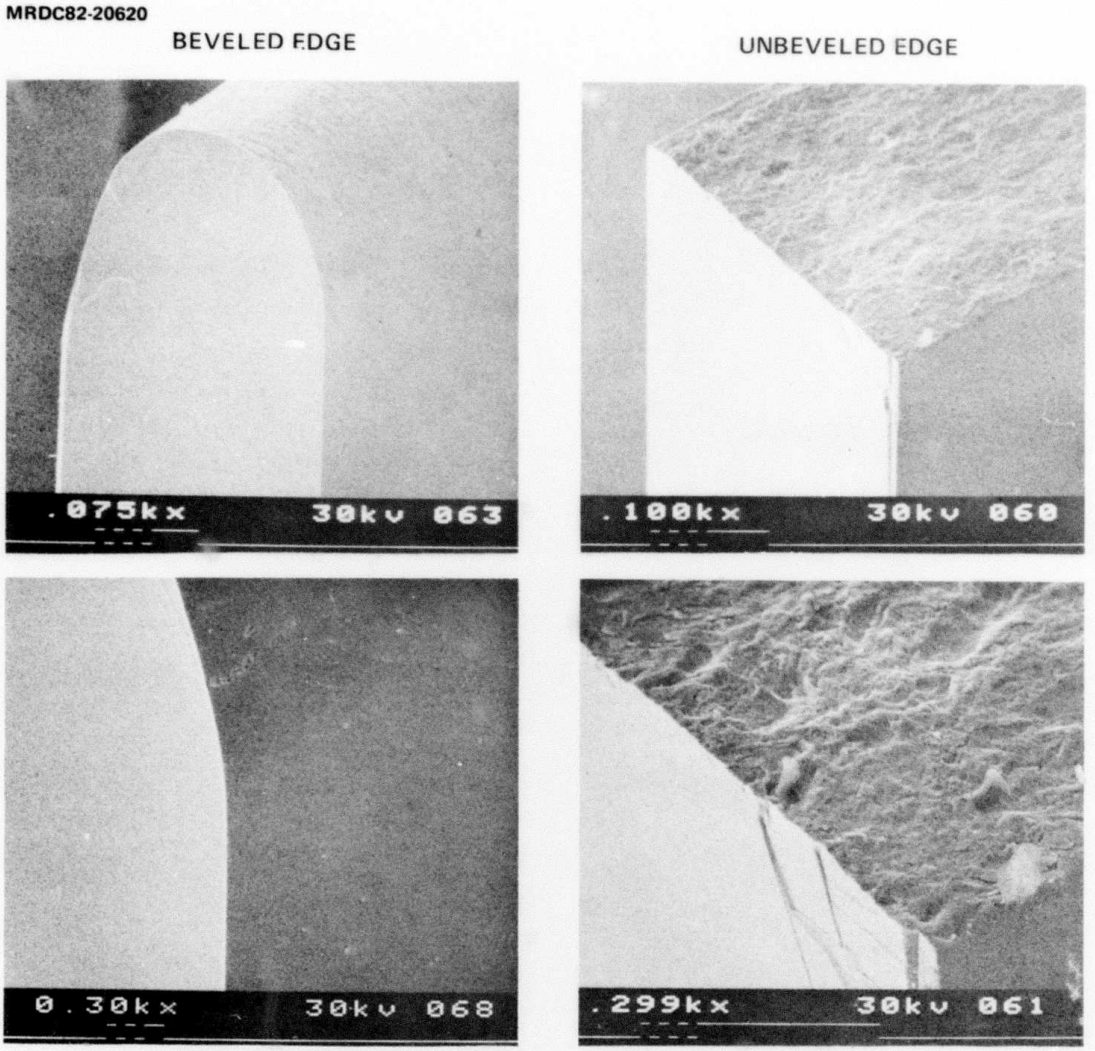


Fig. 2.1-3 Comparison of beveled and unbeveled wafer edges.

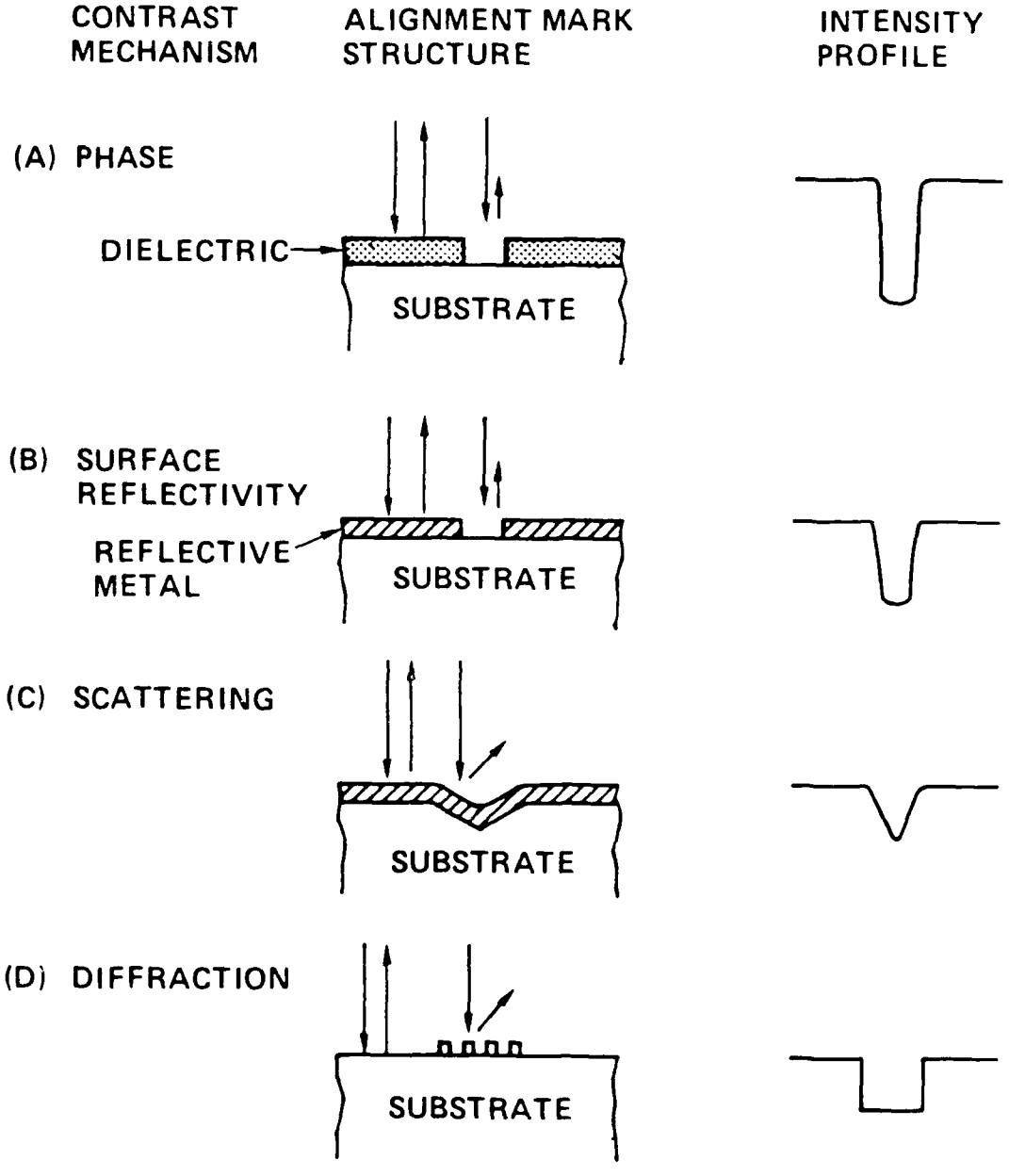
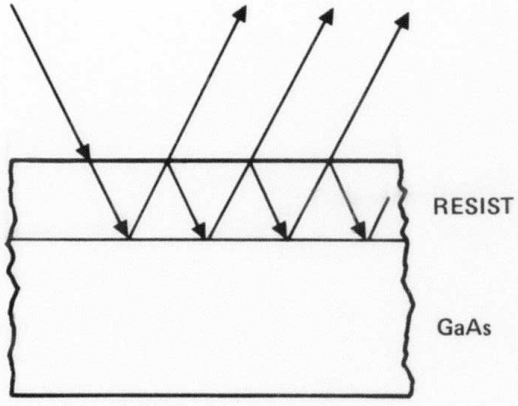
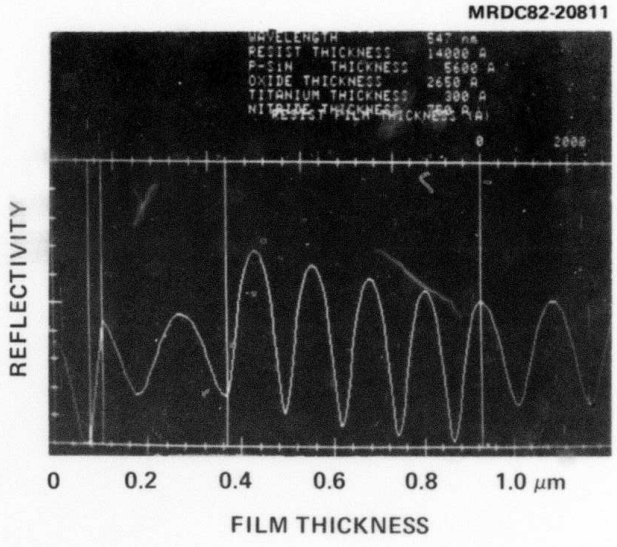
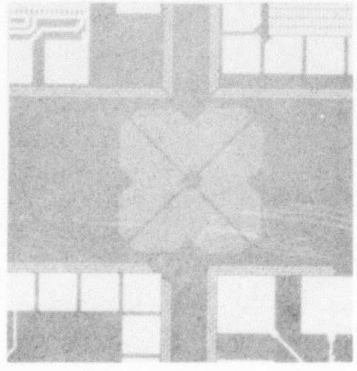


Fig. 2.1-4 Contrast mechanisms for Censor 10X wafer stepper.







ALIGNMENT MARK

AFTER SCHOTTKY METAL STEP

Fig. 2.1-5 Interference effects on alignment mark contrast.

2.2 Test Chip Yield Studies

In order to gain a better understanding of the yield of certain processing steps, a crossover test structure was incorporated into several of the mask sets. This pattern, shown schematicaly in Fig. 2.2-1, was used to evaluate the following yield limiting factors: 1) shorts between various lengths of parallel Schottky metal lines, 2) shorts between various lengths of second level metal lines, and 3) shorts between first and second level metal. The experimental results are shown in Figs. 2.2-2 through 2.2-4. Also shown is the approximate number of crossovers and metal line lengths that are currently being considered for the 1K low power RAM. The tests indicate that processes associated with second level metal, i.e., sputtering, lithography and etching, are more susceptible to defects than the processes associated with first level metal. The fact that first level metal is lifted rather than etched could be an important factor in this regard. The crossover data and the Schottky metal data, on the other hand, are encouraging and demonstrate the feasibility of fabricating circuits at the 1K RAM complexity level.

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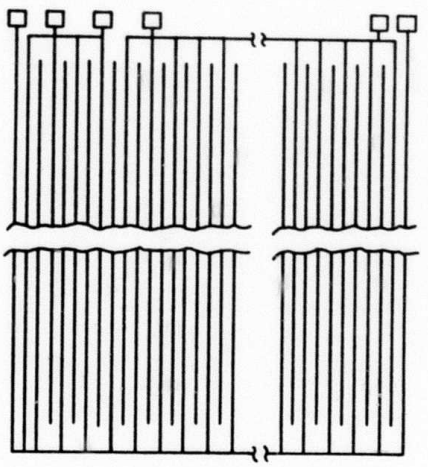

Fig. 2.2-1 Crossover, Schottky metal, and second level metal test structure.

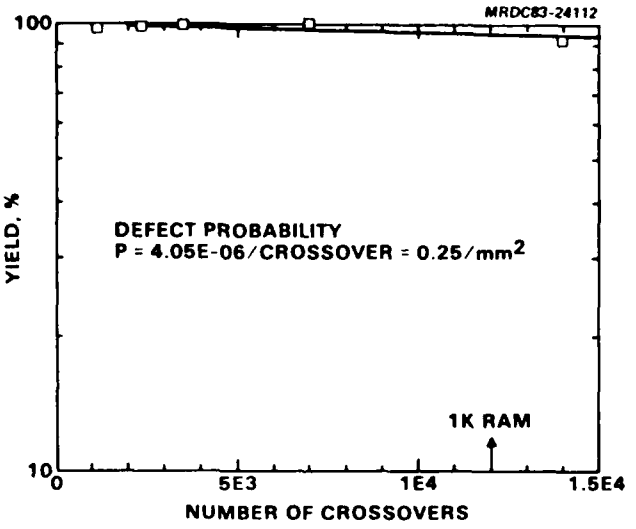

Fig. 2.2-2 Crossover yield.

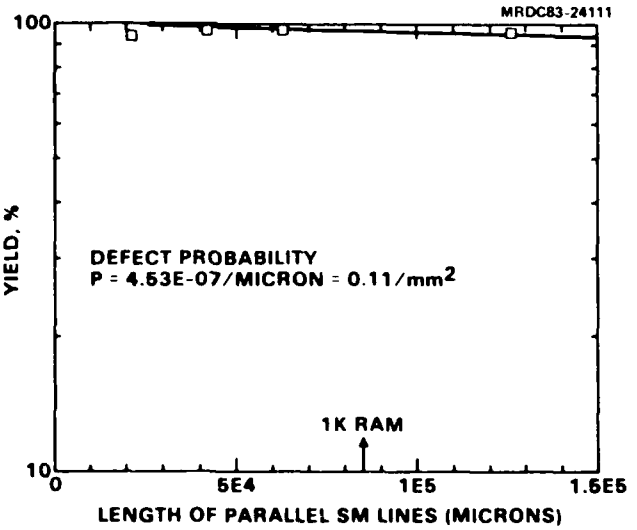

Fig. 2.2-3 Schottky metal yield.

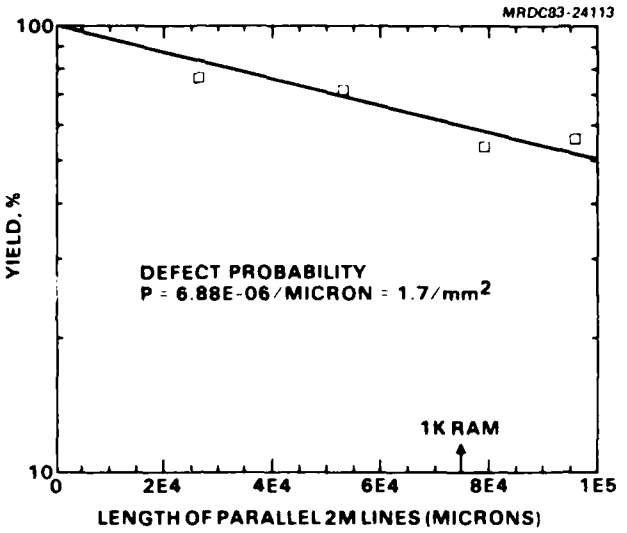

Fig. 2.2-4 Second level metal yield.

2.3 Threshold Uniformity Studies

To obtain high yield consistency for GaAs circuits, maintaining good threshold voltage uniformity across GaAs wafers and minimizing absolute threshold variations on a wafer-to-wafer basis will be necessary. Typically, such variations should be less than 100 mV peak to reach across 3-in. wafer for SDFL (Schottky Diode FET Logic) and BFL (Buffered FET Logic) logic circuits. For enhancement mode devices deviations from the average ultimately should be less than 50 mV peak to peak.

Threshold variations may arise from a number of different sources. For a through-the-cap implant process the thickness of the cap, singular variations of the implant scan, thickness of the native oxide between cap and substrate, and uniformity errors associated with the implant process can significantly affect threshold voltage uniformity. Material properties such as residual acceptor content and dislocation density may also play a significant role. In addition, piezoelectric effects greatly influence threshold voltage values, and thus cap induced stresses must be controlled to the greatest extent possible. The following section describes the results from C-V (Capacitance-Voltage) measurements which were used to analyze implant and capping nonuniformities, as well as a detailed analysis of piezoelectric effects in GaAs.

2.3.1 C-V Measurements

To help determine those factors which influence threshold voltage variations in the standard GaAs IC fabrication process, a simple C-V process was established to help isolate factors which contribute to nonuniformities in threshold uniformity. The process consists of capping a 3-in. wafer with Si_3N_4, implanting the wafer, annealing the wafer, defining a high density array of pseudo-ohmic Schottky diodes across the 3-in. wafer, and measuring the depletion voltage using an automatic wafer stepping system across the entire wafer. The advantages of this simplified process are that: 1) only one mask level is required. This simplifies fabrication, and accelerates the turnaround time; 2) most of the critical fabrication steps in the normal IC fabrication process are included so that the simplified process closely replicates the actual fabrication; 3) complicating factors such as short channel effects or piezoelectric effects which can shift FET thresholds are not present, so they can be effectively separated from activation and implant related nonuniformities; and 4) interpretition of the C-V results can be obtained rapidly in a relatively short period of time for a large density array of points.

Three wafers were processed to establish potential sources of nonuniformity across wafers. The first two wafers received implants of Si and Se at doses of 2.5E12 with energies 130 KeV and 320 KeV, respectively, through a 750Å Si_3N_4 cap. The third wafer was implanted at a 45° angle with respect to axis of the ion beam with Se at a dose of 2.5E12 cm^{-2} at 320 KeV. Figures 2.3-1 and 2.3-2 show 3-dimensional plots across the wafer for the depletion voltage in each of these cases. Figure 2.3-3 shows individual cross sections across the Se implanted wafer.

The first two wafers were processed to compare the overall uniformity between Si and Se implants and to test whether residual dislocations have any influence on the uniformity across wafer. Si might be expected to behave differently than Se since it is an amphoteric dopant. Although the Si does show lower activation across wafer than the Se, the uniformity of each across wafer is comparable. In both cases, however, the uniformity is dominated by a sys-

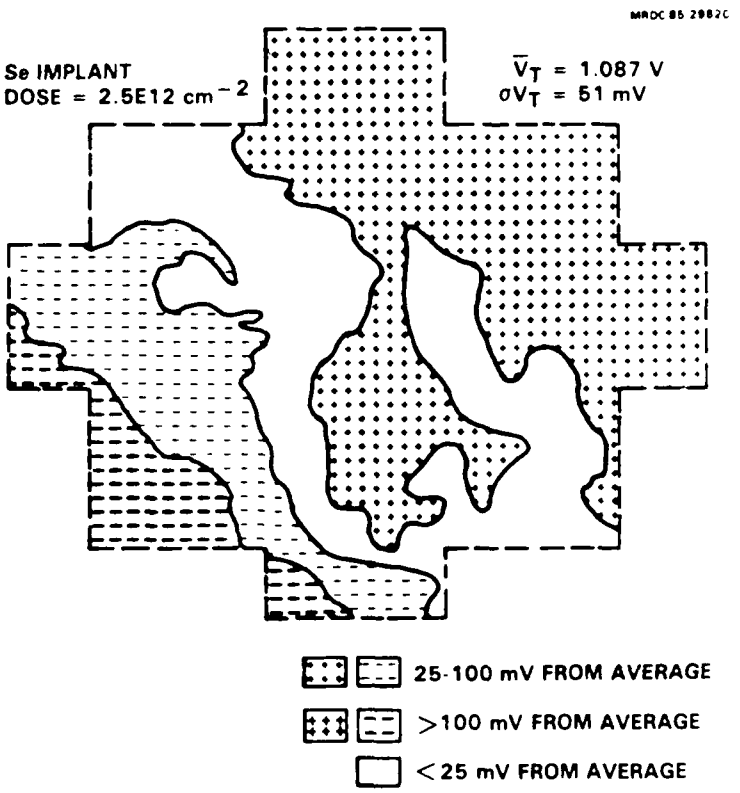

Fig. 2.3-1 Implant uniformity, Se implant.

tematic gradient across the wafer which coincides with the angular orientation of the flat relative to the ion beam. This orientation is chosen to be 7° in order to reduce channeling effects. To test whether the implant uniformity was affecting threshold uniformity, the third wafer was implanted with a 45° rotation about the axis of the wafer. A discontinuity was found in the threshold voltage (vertically oriented in the center of the profile for the first two wafers) rotated by 45°, suggesting that the nonuniformities were associated with implanted nonuniformities rather than material properties.

One important feature illustrated by the C-V data is that most reported LEC material nonuniformities are due to systematic rather than random variations in threshold voltage. The statistical variations in threshold voltage are generally much smaller, being on the order of 20 mV. Standard deviations due to

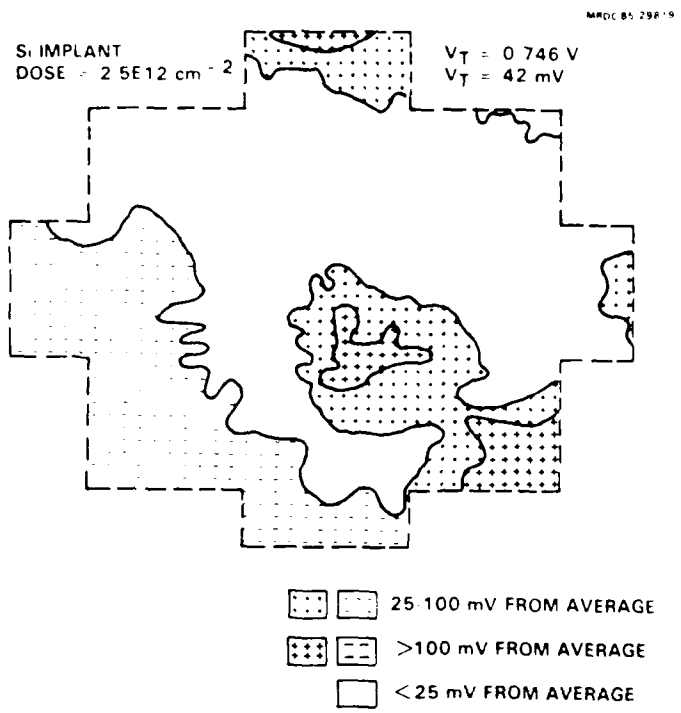

Fig. 2.3-2
Implant uniformity, Se implant.

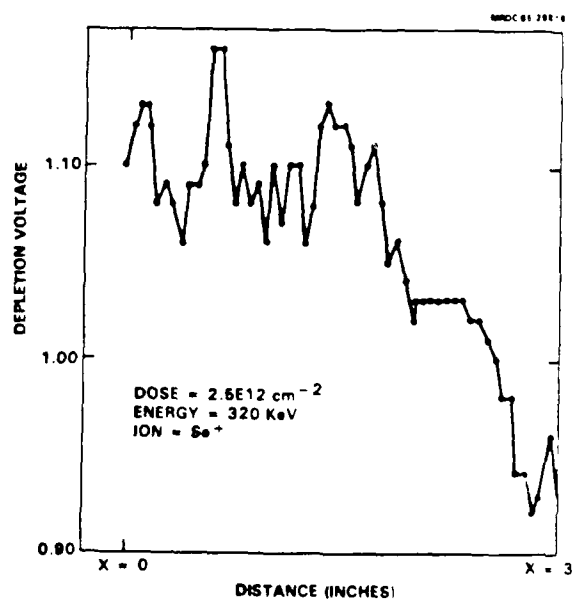

Fig. 2.3-3
Implant uniformity, Se implant.

the larger systematic variations typically have been 50-70 mV. The magnitude of the variations across wafer shown in Figs. 2.3-1 and 2.3-2 are similar to those associated with dislocations by researchers at other laboratories. However, any obvious effects of the dislocations on threshold voltage uniformity have not been observed. Dislocation densities exhibit a distinctive W-shaped pattern in LEC (Liquid Encapsulated Czochralski) material which would be apparent in Figs. 2.3-1, 2.3-2 and 2.3-3. Similar arguments can be made regarding the uniformity of residual impurities in the substrate. The distribution of impurities also typically shows a W-shaped pattern which would be apparent.

Nonuniformities which have a strong dependence on the device area can be ruled out. The deviations of depletion voltage of the C-V dots is comparable to the deviation in threshold voltage of FETs fabricated on similar wafers even though the difference in area is roughly 2000.

2.3.2 Piezoelectrically Generated Device Nonuniformity

It has been shown that the device characteristics of GaAs MESFETs strongly depend on the crystal orientation of the substrate.[1,2] Such dependence can be varied by either device structure or processing techniques. The physical mechanism underlying this phenomenon has been recently found to be the piezoelectric effect.[3] Elastic stresses are often unintentionally introduced into the GaAs substrate during device fabrication. The stresses can be generated during thermal processing, metal contact alloying and, more importantly, from dielectric overlayers.[4,5] The overlayer, such as Si_3N_4 or SiO_2, can stress the underlying semiconductor substrate, and can build up to particularly high values near the openings in the films.[4] The magnitude of the stresses depend on the dielectric deposition technique, but in the vicinity of dielectric openings, the stresses can be as high as 5×10^9 dynes/cm^2.[5] GaAs, unlike Si, is a piezoelectric material. Such high stresses can induce piezoelectric charges causing significant shifts in the threshold voltage of the FETs with certain orientations.[3] Based on this model, the change in the threshold voltage, δV_{th}, can be calculated as

$$\delta V_{th} = \frac{1}{\varepsilon} \int_0^{W_{max}} z\rho_{pz}(z)dz + \frac{q}{\varepsilon} W_{max} n_{ch}(W_{max}) \delta W_{max} \quad , \qquad (1)$$

where ρ_{pz} is the stress-induced piezoelectric charge density, z is the distance from the surface, W_{max} is the depth of the channel, and n_{ch} the carrier concentration in the channel. The first term of Eq. (1) is caused by either accumulation or compensation of channel carriers with the piezoelectric charges, the second term of which is caused by the channel depth modulation due to the accumulation or compensation. The magnitude of ρ_{pz} is determined by the substrate crystal structure, the thickness of the dielectric overlayers, and the length of film openings.

Figure 2.3-4 illustrates the orientation effect for "capped" (Si_3N_4) GaAs substrates, where drain current vs gate voltage is plotted for five different FET orientations. It clearly shows that the device characteristics are a function of the orientation, θ. The current and the threshold voltage increase continuously with angle θ, where θ = 0 corresponds to the [011] directions.

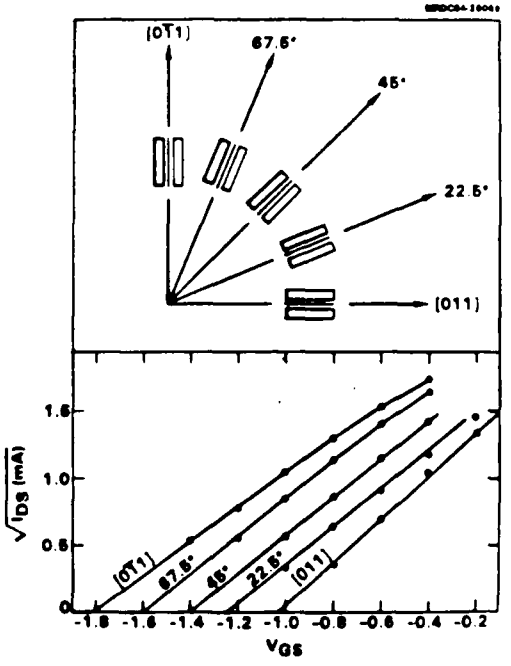

Fig. 2.3-4
Orientation effect for Si_3N_4 capped GaAs wafers.

Utilizing test FETs on the AR7 wafers, saturation currents (I_{dss}) and threshold voltages (V_{th}) for the different orientations were measured as a function of their radial position. It was found that devices have a strong radial dependence characteristics of either the [011] or [01$\bar{1}$] directions. As shown in Fig. 2.3-5, FETs along the [01$\bar{1}$] direction always have higher threshold voltages than their [011] counterparts. The radial dependence of device characteristics is opposite in these two directions. Threshold voltage increases with radius for [011] FETs, but decreases for [01$\bar{1}$] FETs. The difference in threshold voltage between [011] and [01$\bar{1}$] FETs can be considerable, with V_{th} as high as 0.7 V at the center of the wafer, and as low as 0.2 V at the edge. Measurement of the saturation currents also reveals a similar radial dependence. Plotting $|V_{th}|$ as a function of FET position on a 3 inch wafer, the opposing radial dependence between [011] and [01$\bar{1}$] FETs could be demonstrated, as shown in Figs. 2.3-6a and 2.3-6c. On the other hand, the [010] and [001] FETs have identical

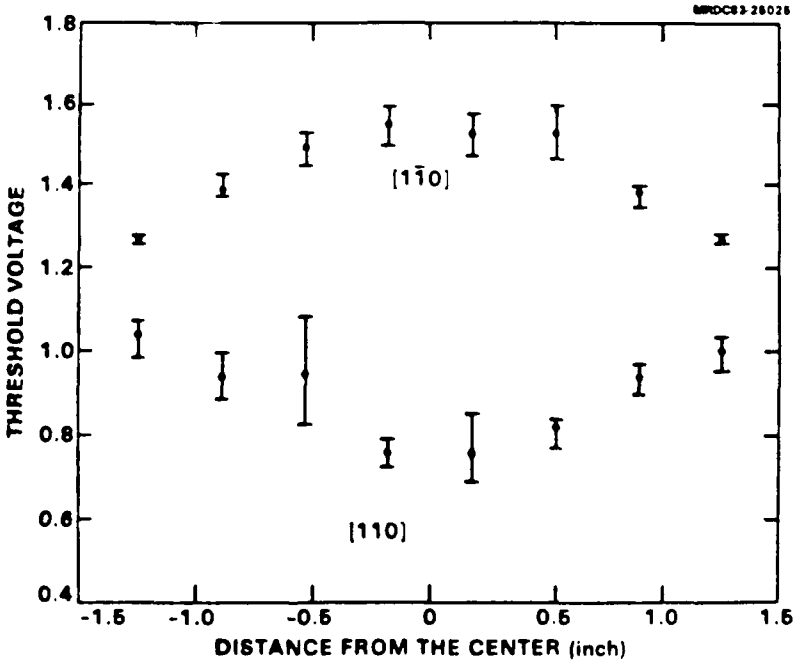

Fig. 2.3-5 Radial dependence of threshold voltage.

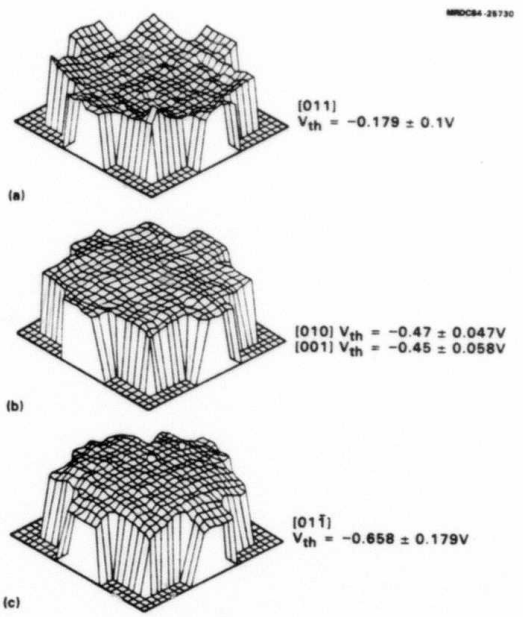

Fig. 2.3-6 Threshold uniformity plots: (a) [011], (b) [010], (c) [01$\bar{1}$].

characteristics and do not show any radial dependence. This case is shown in Fig. 2.3-6b. The values of I_{dss} and V_{th} of the [001] and [010] FETs are about half the values of [01$\bar{1}$] and [011] FETs. In a typical example, the average threshold voltage of the [011] FET is -0.179 V with a standard deviation of 100 mV; the perpendicular [01$\bar{1}$] FET has an average threshold of -0.658 V and 179 mV standard deviation. The corresponding average and standard deviation for [010] FETs is -0.47 V and 47 mV, respectively, and for the [001] FETs is -0.45 V and 58 mV. Because of the lack of radial dependence, both [001] and [010] FETs have half the standard deviation of their [01$\bar{1}$] and [011] counterparts.

The orientation dependence of the radial distribution of FET characteristics can be explained by the piezoelectric effect. The stresses produced by the dielectric film deposited on the surface of the device can induce a piezoelectric charge density, ρ_{pz}, in the active channel causing the threshold voltage to shift. When the piezoelectric charge density $\rho_{pz}(W_{max})$ is much smaller

than $n_{ch}(W_{max})$, the second term of Eq. (1) is not significant and the deviation of threshold voltage is proportional to the first term in Eq. (1); as $\rho_{pz}(W_{max})$ approaches $n_{ch}(W_{max})$, the second term increases very rapidly and dominates.

Because of the anisotropy of GaAs crystals, ρ_{pz} induced in the channels of [011] FETs is of opposite sign to that in the [01$\bar{1}$] FETs, and it vanishes for the FETs in [001] and [010] directions. In the channels of [011] and [01$\bar{1}$] FETs, the magnitude of ρ_{pz} is proportional to the thickness of the dielectric overlayers, and approximately inversely proportional to the square of the length of the film openings in the gate area.[3] This is why the orientation dependences of the FETs characteristics are observed. Since the piezoelectric charges are induced by the stresses from the dielectric film on the surface, ρ_{pz} is strongly dependent on the processing parameters. Variations in the thickness of the dielectric film and in the size of the film openings for gate deposition may have very strong influences on the value of ρ_{pz}. For large diameter GaAs wafers, radial dependences of these processing parameters are sometimes difficult to avoid. The deposited dielectric films are generally thinner around the wafer edge and thicker in the center of the substrate. In addition, the amount of undercut of the dielectric openings by plasma etching also often appears to be radially dependent.

Evidence that the threshold voltage shifts are caused by stresses can be found in the measured values of threshold shift for different thicknesses of dielectric overlayers, as seen in Fig. 2.3-7. Here, the threshold voltages of the FETs oriented at angles of 0°, 22.5°, 45°, 67.5° and 90° with respect to the [011] direction were measured as the surface Si_3N_4 film was thinned by CF_4 plasma etching. Before the Si_3N_4 was removed, the dependence of the threshold voltage on orientation angle was distributed as expected from theoretical considerations.[3] The 90° FET had a threshold voltage of 1.8 V, which was nearly two times that of the 0° FET. As the Si_3N_4 layer was gradually removed, the threshold voltages of the FETs oriented at angles smaller than 45° increased, while the threshold voltages of the FETs oriented at angles larger than 45° decreased. The largest changes occurred for 0° and 90° FETs, and the 45° FETs had nearly no change in threshold voltage. This result clearly indicates the stress dependence of the orientation effect. The characteristics of the 45°

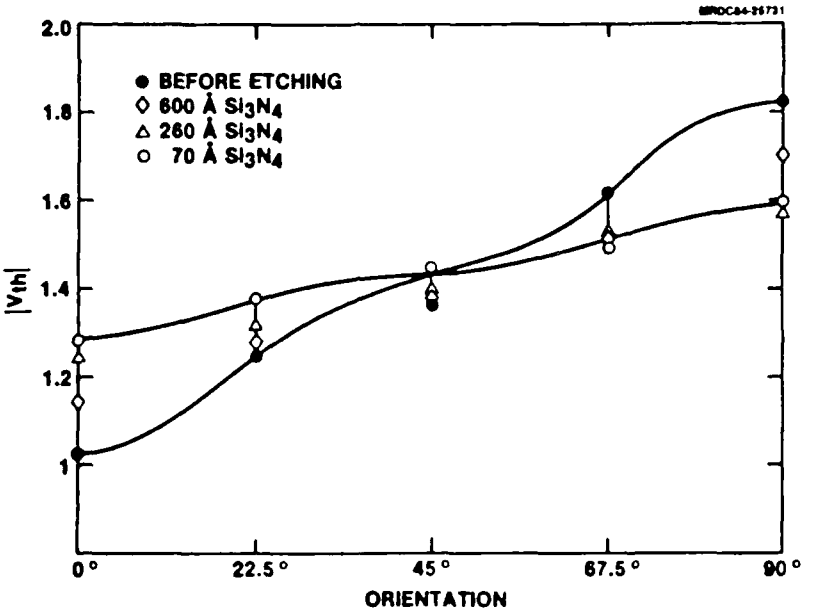

Fig. 2.3-7 Effect of dielectric etching on threshold voltage.

FETs or the FETs oriented in [010] or [001] directions are obviously not as process dependent as those of the [011] and [01$\bar{1}$] FETs. Therefore, unless the radial dependence of the process nonuniformity can be totally eliminated, it is desirable to choose a FET orientation in which process-induced effects on the device characteristics are minimized. Another advantage of using [010] and [001] FETs is increased packing density. Because the device characteristics of these two kinds of FETs are identical, it is not necessary to have all the FETs in a circuit oriented in the same direction to minimize variations.

2.4 Materials Characterization

The emphasis of the materials development programs has shifted from the basic issue of growing semi-insulating GaAs by the liquid encapsulated Czochralski (LEC) technique to the "fine tuning" of material properties for integrated circuit applications. One of the current objectives is to increase the yield of qualified material for IC processing. To achieve this goal, more emphasis has

been placed on gaining tighter control over the predominant electrical centers, such as carbon and EL2, and improving the uniformity of these centers throughout the crystal. For example, it has been found that thermal annealing of bulk GaAs leads to improved uniformity of the radial EL2 distribution. In addition, techniques have been developed to reduce the background carbon concentration to the 10^{14} cm^{-3} level, a factor of 5-10 improvement over conventional LEC material. It is anticipated that this reduction will lead to better control over FET threshold voltage, V_T, as discussed below.

At least two mechanisms have been shown to influence axial (wafer-to-wafer) uniformity of FET threshold voltage along undoped semi-insulating LEC ingots. On the one hand, carbon* segregation during crystal growth leads to an increase of the carbon concentration toward the last portion of the crystal to solidify (tail). Since carbon is an acceptor, the corresponding FET threshold voltage profile increases toward the tail. On the other hand, a second mechanism has the opposite effect of carbon and actually counterbalances the carbon-controlled profile. This mechanism was uncovered in studies of ultra-low carbon GaAs.

One possible explanation for the second mechanism is outdiffusion of transition metal acceptors from the bulk of the substrate material and accumulation in the implanted layers. Annealing experiments were conducted to evaluate methods of damage gettering to reduce the metal concentration in active layers and to improve the reproducibility of the implant process.

Ultra-low carbon material ($< 8 \times 10^{14}$ cm^{-3}) was used in the first set of annealing studies. One-inch squares were obtained from as-sliced wafers from the seed end and tail of the crystal. The samples were heated for 4 h at 850°C. After cooling, the samples were lapped and polished. C-V depletion voltage measurements were made by a standard technique on as-grown and annealed samples. Twenty data points were taken on each sample.

*Carbon is a predominant background acceptor in LEC GaAs.

A comparison of C-V depletion voltages at the seed end and tail of the as-grown and annealed samples, given in Table 2.4-1, shows that the 200 mV depletion voltage difference along the crystal was virtually eliminated after annealing and that exceptionally high uniformity was achieved. These results could be explained because transition metals such as Fe were gettered to the saw damage induced by the annular I.D. saw and were removed by subsequent polishing steps.

Table 2.4-1
Effect of Annealing on Threshold Voltage Uniformity LED Ingot*

	Depletion Voltage (Volts)	
	Seed End	Tail End
As-Grown	1.47	1.27
Annealed	1.41	1.41

*Low-Carbon Ingot

As a result of this experiment, another annealing series was conducted using samples from three different crystals containing low (R88), medium (R99), and high (R84) carbon levels, respectively. The carbon concentration and the depletion voltages before and after annealing are given in Table 2.4-2.

Based on the first annealing experiment, two results were anticipated. First, the seed-to-tail uniformity of the low carbon crystal was expected to improve. However, the observed 50 mV improvement (200 mV difference as grown vs 150 mV after annealing) is small compared to the change observed in the first experiment. Second, the threshold voltage was expected to increase at the tail of all crystals after annealing. In fact, all three values decreased.

The apparent irreproducibility of the annealing experiments does not necessarily mean that transition metals do not play a role in controlling the

Table 2.4-2

Effect of Annealing on Threshold Voltage Reproducibility

Crystal No.	Carbon Concentration (cm^{-3})	Ave. Depletion Voltage (Annealed), (V)	Ave. Depletion Voltage (As-Grown), (V)	DV (As-Grown)-(Annealed), (V)
88-4	U.D.*	1.35	1.43	0.08
88-53	U.D.	1.20	1.23	0.03
ΔDV (Tail Seed)		-0.15	-0.20	
99-1	4.4×10^{15}	1.18	1.09	-0.09
99-61	U.D.	0.97	1.07	0.10
ΔDV (Tail Seed)		-0.21	-1.02	
84-5	3.4×10^{16}	0.55	0.69	0.14
84-45	1.2×10^{16}	1.01	1.04	0.03
ΔDV (Tail Seed)		0.46	0.35	

*U.D. = undetermined.

threshold voltage level of implanted layers. In fact, SIMS (Secondary Ion Mass Spectroscopy) chemical analysis of the material annealed in the first experiment (Table 2.4-1) indicated an unusually high concentration of manganese. Therefore, the effect of annealing could be accounted for by manganese gettering. However, this same mechanism is not consistent with the ineffectiveness of annealing of crystal R88, notwithstanding possible variations of the annealing process itself. The central conclusion to be drawn from this work is that a more quantitative approach to evaluating transition metals is needed during routine processing. The application of DLTS (Deep Level Transient Spectroscopy) would seem to be a preferred method. However, a quantitative measure of hole traps would require p-type implants, which would be difficult to implement.

3.0 GATE ARRAY DEVELOPMENT

The two mask sets used for gate array development have the designation AR7 and AR8. The AR7 mast set was the first attempt to design and fabricate a configurable cell array, and thus, required numerous test structures to evaluate cell design and interconnect options, as well as to evaluate the effect of interconnect loading on cell characteristics. Also included in this mask set was a 5 × 5 multiplier as a demonstration circuit. The AR8 mask set was an extension of AR7 and, as such, used the same basic cell design. The demonstration circuits were increased to the 1K equivalent gate complexity, and were used to evaluate yield for large area chip designs. The following two sections describe each of these mask sets along with the resultant testing evaluations.

3.1 AR7 Mask Set

Several factors influence the design of a GaAs gate array. As with most designs, several of the design parameters interact with one another, yielding several possible solutions to the design goals. The parameters which dominate the design of the gate array are the cell power consumption, cell complexity, cell logic type and groupings of the cells. The following section will address basic cell design, interconnect issues, and the resultant mask layout. Also included are the test results for ring oscillators and the 5 × 5 multiplier.

3.1.1 Design Considerations

In order to maintain an acceptable power dissipation factor for a large (4K) gate array, the average power per gate must be ~ 1 mW. Included in this average power per gate is the input/output (I/O) cell power consumption. Unlike most custom integrated circuit designs, the gate array power consumption varies according to the number of cells of the array which are used in implementing a desired logic function. Hence, the cell utilization factor which has a practical upper limit of ~ 90% can allow for a slightly higher power per gate factor.

The second design parameter is the complexity of a single cell within the gate array. At the low end of the spectrum is a cell composed of either a two-input NOR, or a two-input NAND gate. From there, a complexity increases to multi-input NOR, or multi-output type cell arrangements. It is difficult to quantitatively assign a number to the cell complexity factor. One method which is used is to construct several logic functions with two-input NAND gates (or two-input NOR gates) and then construct these same structures with cells. The average ratio between the number of two-input gates to the number of cells needed to construct the desired function is the gate equivalent factor. The factor can typically range from a value of 1 to 3, depending on the cell configuration and complexity. The higher the gate equivalent factor, the lower the number of cells necessary to implement a given gate array size.

The cell logic type corresponds to the selection of one of the available logic families in GaAs IC design. The four types which were considered were SDFL, programmable output SDFL, FL and BFL. As expected, each of these logic types exhibited both advantages and disadvantages over one another. The final line choice for the GaAs gate array was BFL. BFL was selected for several reasons. First, and foremost, is the fact that the BFL structure has essentially zero dc input bias current. This makes BFL immune from dc fanout limitations which can affect SDFL. Next, BFL is less sensitive to process variation. This factor arises due to the proximity of the source follower and pull-down current source of a BFL circuit. The major disadvantages of BFL, when compared to other logic types, are the high input capacitance and high power consumption. However, the high input capacitance is insignificant when compared to the interconnect line-to-line and crossover capacitance. Thus, BFL input capacitance is not a major disadvantage. The high power consumption of BFL can be alleviated by implementing a scheme which allows for the programming of the output transistor sizes. This would allow for the selection of a low drive for short interconnections and the selection of a high drive for long interconnections.

The grouping of the cells is also a factor to consider when designing the gate array. The cells can be grouped from a cluster of only one to a clus-

ter of several cells. Examining both extremes yields some insight into the problem. If a cluster is selected with only one cell, there is a minimum distance of at least one track width between cells. This is not an attractive arrangement. Next, if the cells are clustered into large groups with all of the interconnecting channels on the perimeter, few and probably no channels would be available internally to the grouping. Thus, the best solution is in between a grouping of one to a grouping of several cells. The solution finally arrived at came as a result of several iterations between the cell design done at Rockwell and the automatic cell placement and routing software development being done at Mayo Foundation.

3.1.2 Cell Design

The results of a thorough examination of the design goals and objectives yielded a basic cell design, as shown in Fig. 3.1-1. The cell is a four-input BFL gate. The circuit is mask programmable to perform one of the nine logic functions, shown in Fig. 3.1-2. The design also allows for the selection of a low or high output drive capability. The high drive option is obtained by paralleling transistors Q6A, Q6B and Q7A, Q7B.

The layout of a single basic cell is shown in Fig. 3.1-3. The basic cell is 31 x 53 μm^2. Extra Schottky metal and vias are included in the basic cell design to allow for the implementation of all nine logic functions.

After several iterations, it was determined that a grouping of two basic cells would yield the best gate array peformance. A layout of this grouping is shown in Fig. 3.1-4. The layout allows for multiple input/output entrances and exits to the cell. Also, cross-coupling between basic cells can be accomplished without having to run interconnects externally to the cell. Both of these factors yield a compact interconnect of the gate array. An interconnect example of two basic cells is shown in Fig. 3.1-5.

All of the programming of the cells logic function and the selection of low/high output drive capability is done with only one layer of metalization. The reasoning behind this is the following. There are currently two layers of

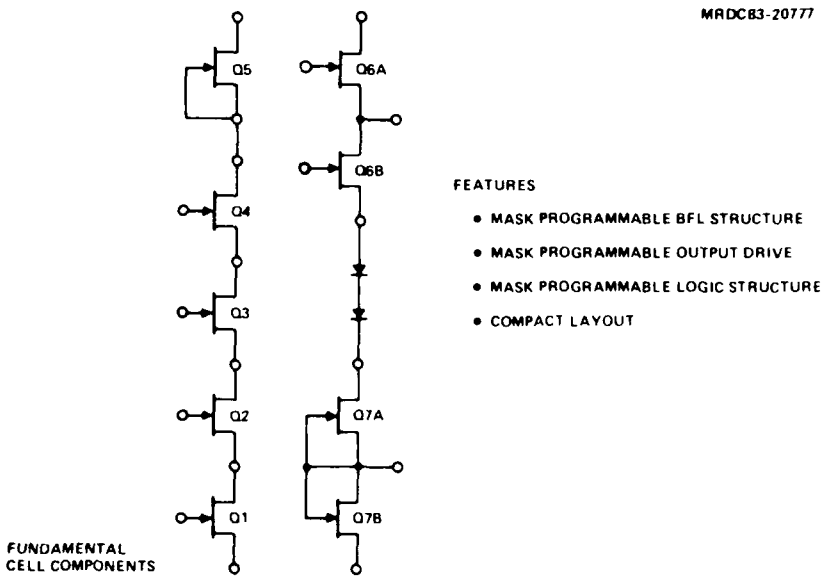

Fig. 3.1-1 GaAs gate array basic cell design.

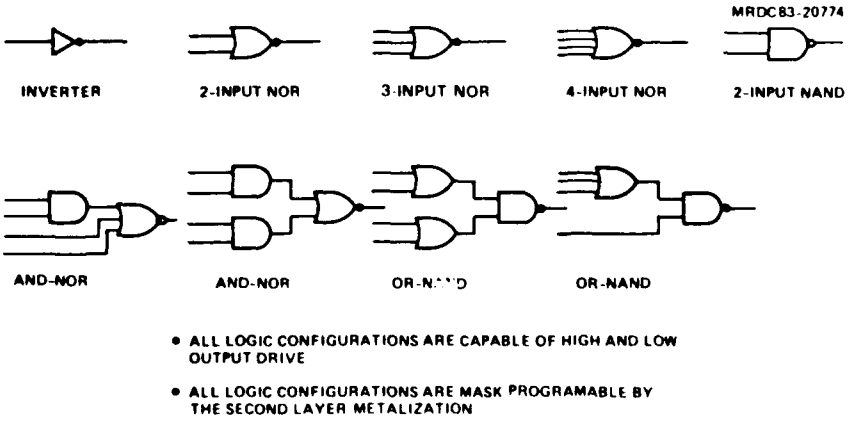

Fig. 3.1-2 GaAs gate array basic cell logic capabilities.

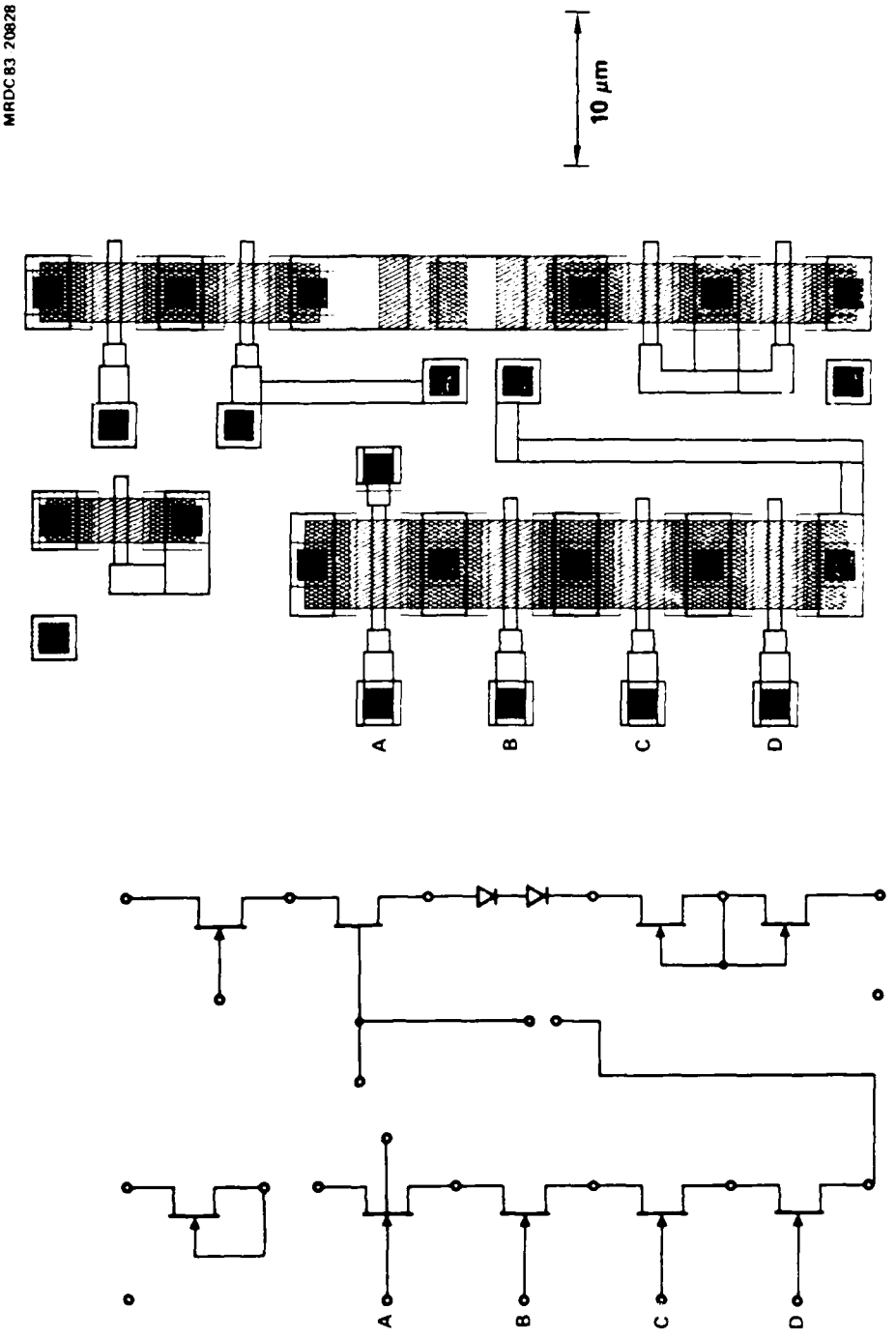

Fig. 3.1-3 GaAs gate array basic cell schematic and layout.

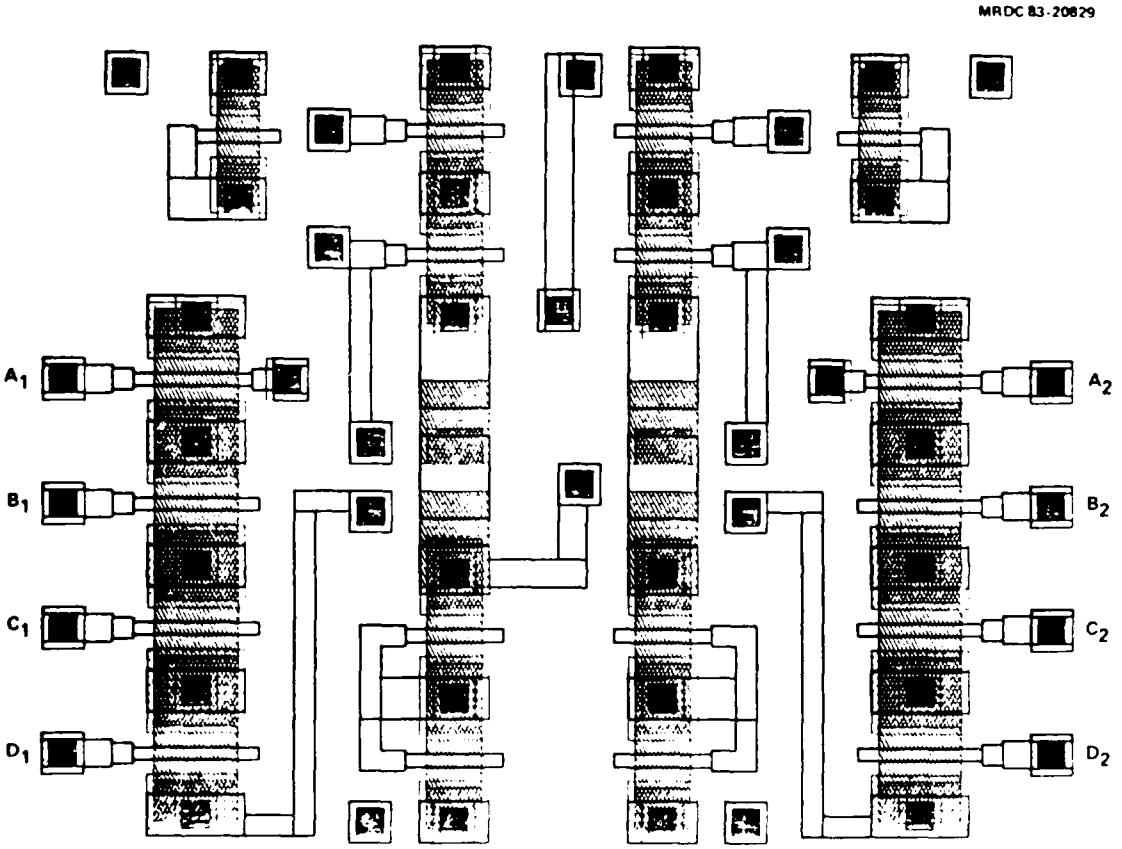

Fig. 3.1-4 Grouping of two basic cells.

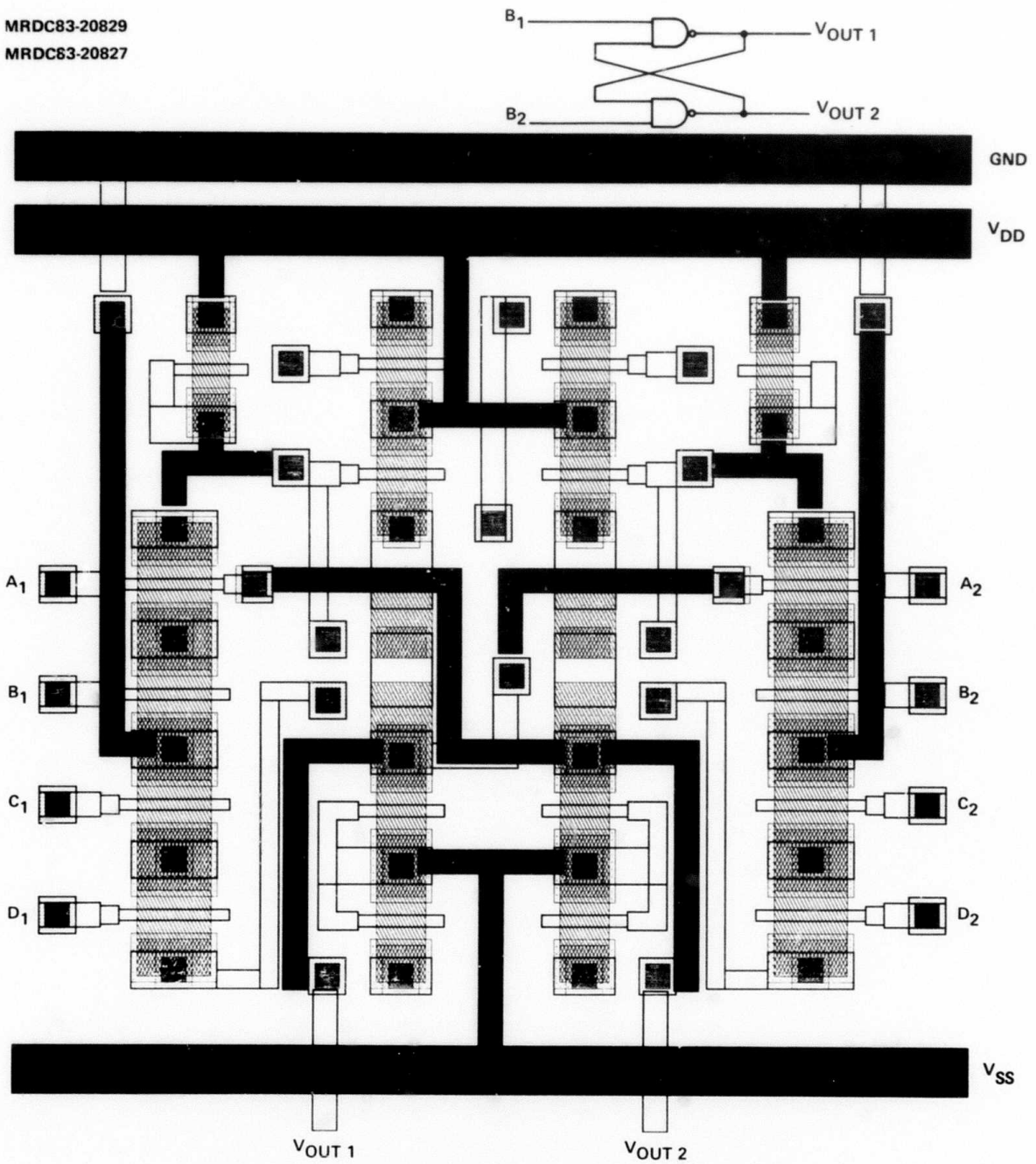

Fig. 3.1-5 GaAs gate array cell programming.

metalization available for programming, namely, first layer metalization and second layer metalization. Both layers are utilized to program the cell externally, but only the second layer is used internally to the cell. Thus, when a three layer metalization process is developed and implemented, the one major change to the design will be the mapping of the first layer metalization used for interconnects into the third layer. This mapping can be done very easily.

3.1.3 AR7 Mask Design

The AR7 mask contained several circuits to evaluate the BFL gate array. These circuits supplied insight into gate delays, power requirements and device sizes. A MSI level of integration was also included using several gate array cells. This MSI device verifies the performance of the gate array at a large scale level. The rest of the circuits were test structures and miscellaneous devices. The mask layout is shown in Fig. 3.1-6.

Several ring oscillators were included in the AR7 mask design. Their primary purpose was to characterize device speed as a function of operating parameters. The fundamental ring oscillator consists of a 15-stage unloaded ring oscillator with a fanout of one. Several additional versions which have increased loading were included. The loading takes the form of parallel lines, crossovers and fanout. To examine the effects of device size selection, several different size devices within the ring oscillator were selected. The layout of a typical ring oscillator test structure is shown in Fig. 3.1-7.

A large gate array grouping was also included on the mask set. This MSI level of integration includes 306 basic cells and 10 input/output cells. The demonstration circuit for this MSI implementation was a 5 x 5 bit parallel multiplier. Two versions of this multplier were included on the mask set. One employs an exclusively low drive connection of all of the 306 basic cells, while the other employs a high drive connection.

Numerous test structures were also included in the mask, and were used to examine the transfer curves of several cell configurations. These curves verify correct operating conditions and noise margins of the BFL cells. The

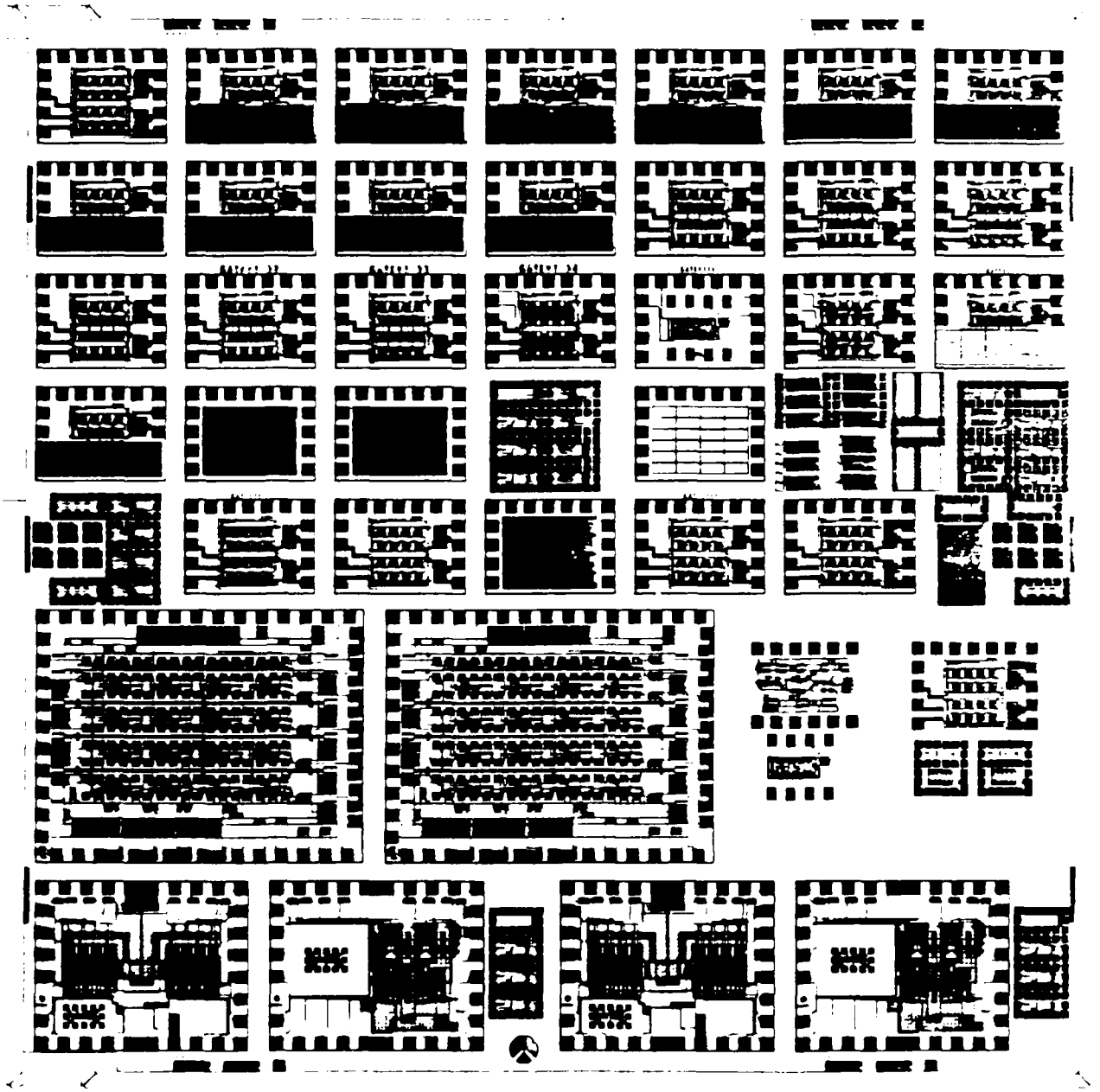

Fig. 3.1-6 Mask set AR7 - gate array design.

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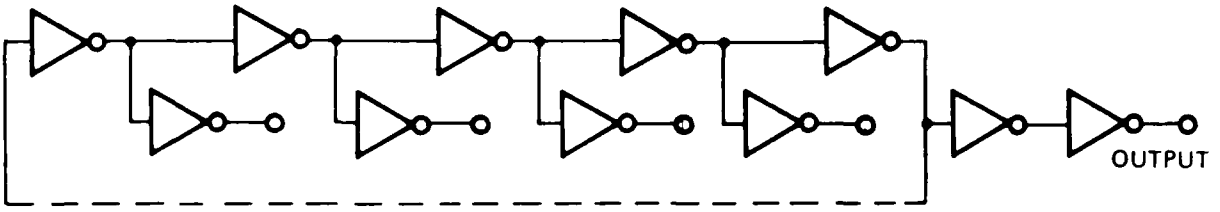
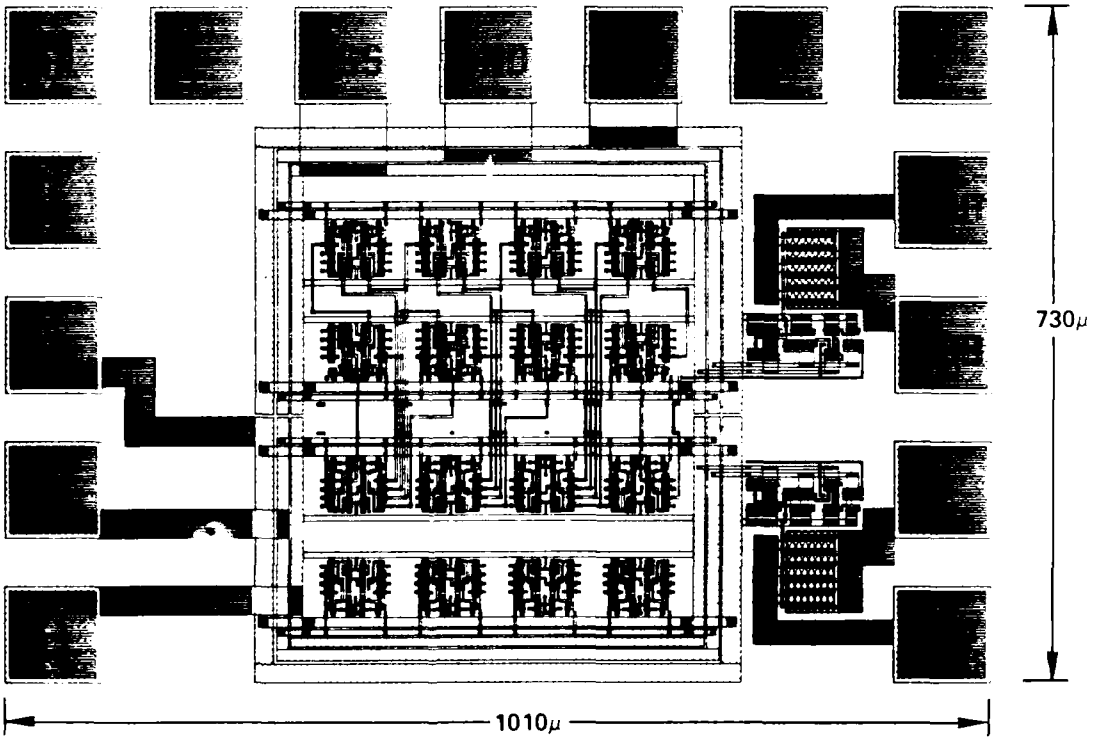
LOGIC DIAGRAM



TEST STRUCTURE LAYOUT



- 15 STAGE RING OSCILLATOR WITH LOADING
- FANOUT = 2

Fig. 3.1-7 GaAs gate array cell characterization test structure.

test structures also include interdigitated line structures to measure line-to-line capacitance and large crossover test structures. All of the test structures emulate actual gate array design dimensions in order to accurately replicate the actual operating conditions.

Two interconnect protocol test chips were included on the mask set. These chips are part of another DARPA-sponsored device development program.

Finally, the AR7 mask set was generated with two Schottky metal levels. The extra mask was included to select between the standard two-diode, -1 V threshold voltage design, while the other is used for the -0.5 V threshold, one-diode design.

3.1.4 DC Test Results

The initial testing to be performed on any newly designed logic family is to examine the transfer curves of a single logic gate. The testing of a logic gate at dc verifies two important parameters. First, the absolute input and output logic voltages can be recorded and compared to predicted results. Next, the noise margin of the designed cell can be examined.

The AR7 wafers have several test structures which can be used to generate the dc transfer curve of the basic cell. Once the single cell transfer curve is obtained, absolute logic levels and noise margins can be measured quantitatively. Using the definitions described in Fig. 3.1-8, the noise margin for several cell configurations were measured. The results of this testing are shown in Figs. 3.1-9 and 3.1-10. These results show that for the device sizes selected, adequate noise margins were obtained for a valid logic family using the BFL logic gates. The worst case noise margin measured was 300 mV, which is excellent for systems applications.

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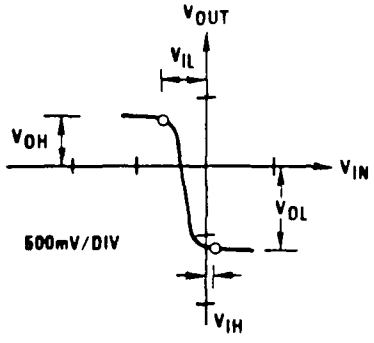

TYPICAL BFL
TRANSFER CURVE

- V_{IL} = INPUT LOGIC LOW VOLTAGE YIELDING A VALID LOGIC OUTPUT VOLTAGE
- V_{IH} = INPUT LOGIC HIGH VOLTAGE YIELDING A VALID LOGIC OUTPUT VOLTAGE
- V_{OL} = OUTPUT LOGIC LOW VOLTAGE
- V_{OH} = OUTPUT LOGIC HIGH VOLTAGE

DEFINITIONS

$V_{NH} = V_{OH} - V_{IH}$
$V_{NL} = |V_{OL} - V_{IL}|$

Fig. 3.1-8 GaAs gate array BFL noise margin definitions.

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INPUT STATE SETUP A B C D	V_{IH} (mV)	V_{OH} (mV)	V_{IL} (mV)	V_{OL} (mV)	V_{NH} (mV)	V_{NL} (mV)
G G L L	-250	650	-600	-1,200	900	600
L L G G	-200	650	-400	-1,200	850	800
G G G G	-300	700	-800	-1,200	1,000	600
G L L L	0	700	-700	-1,200	700	600
L L L G	100	700	-500	-1,200	600	700
WORST CASE	100	650	-700	-1,200	550	600

- V_{DD} = 2.5, V_{SS} = -1.5
- G = GENERATOR INPUT
- L = LOW LEVEL LOGIC INPUT
- WAFER NO. 1-3, DEVICE NO. 8
- V_p = -0.75 V

SCHEMATIC/LAYOUT

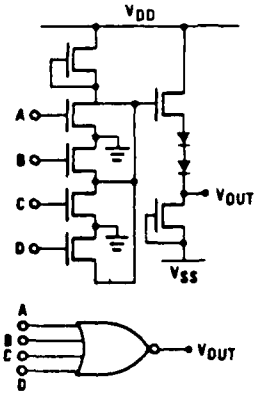

Fig. 3.1-9 GaAs gate array noise margins for various circuit configurations.

V_{DD}/V_{SS} (V)	INPUT STATE SETUP A	B	C	D	V_{IH} (mV)	V_{OH} (mV)	V_{IL} (mV)	V_{OL} (mV)	V_{NH} (mV)	V_{NL} (mV)
2.5/-1.5	G	G	G	G	150	700	-550	-1,200	550	650
	G	G	L	L	350	700	-500	-1,100	350	650
	L	L	G	G	400	700	-550	-1,100	300	650
2.0/-1.0	G	G	G	G	0	300	-550	-800	300	250
	L	L	G	G	250	300	-400	-800	50	400
	G	G	L	L	250	300	-400	-800	50	400

- G = GENERATOR INPUT
- L = LOW LEVEL LOGIC INPUT
- WAFER NO. 1-3, DEVICE NO. 9
- V_p = -0.75 V

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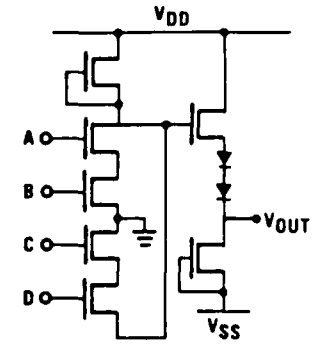
SCHEMATIC/LAYOUT



LOGIC DIAGRAM

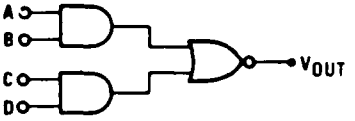


Fig. 3.1-10 GaAs gate array noise margins for various circuit configurations.

3.1.5 Ring Oscillator Test Results

Ring oscillators were used to examine the dynamic performance of the gate array cells. The measurements were made by examining the output frequency of several ring oscillators under different load conditions. In general, the ring oscillator results were as expected, where the average gate delay was in proportion to the output loading. The gate delay also varied with the device sizes; large devices yielded faster gates with lower propagation delays, while smaller devices produced larger delays. The tradeoff in device size selection was not only speed, but also the power consumption.

The first set of ring oscillator measurements was done to examine the gate delay for unloaded ring oscillators. Figures 3.1-11 and 3.1-12 detail the results of these measurements for several device samples. All of the test results are the average values of a sample size of 22 or greater. As expected, the cell speed and power increased with increasing device size.

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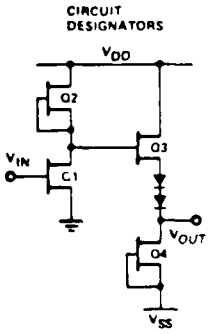

CIRCUIT NO	Q1, Q2, Q3, Q4 (WIDTH, μm)	$\bar{\tau}_D$ (PSEC)	$\bar{P}_D$ (mW)	$\bar{\tau}_D \times \bar{P}_D$ (fJ)
11A	6, 3.5, 4, 4	237	0.87	207
11B	6, 3.5, 6, 6	218	1.57	342
56A	6, 3.5, 4.5, 4	242	0.83	200
56B	6, 3.5, 5, 4	259	0.91	234

- RESULTS FROM 15-STAGE RING OSCILLATOR MEASUREMENTS
- WAFER NO. 1-3
- V_p = 0.86 V
- $\bar{\tau}_D$ AND $\bar{P}_D$ ARE THE WAFER AVERAGE VALUES

Fig. 3.1-11 GaAs gate array ring oscillator test results.

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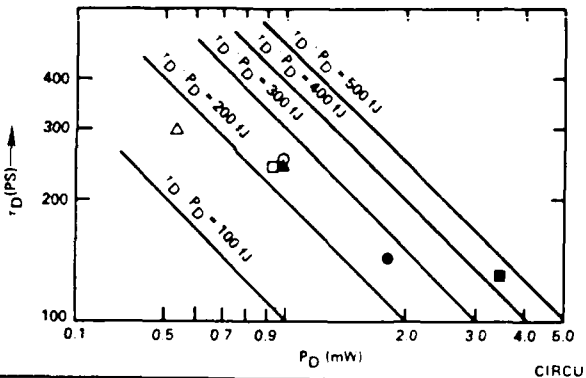

CIRCUIT NO.	Q1, Q2, Q3, Q4 (WIDTH, μm)	$\bar{\tau}_D$ (PS)	$\bar{P}_D$ (mW)	$\bar{\tau}_D \times \bar{P}_D$ (fJ)
53A → △	4.5, 2.5, 3, 3	300	0.54	162
56A → ○	6, 3.5, 4, 4.5	243	0.94	228
53B → □	4.5, 2.5, 6, 6	263	1.00	263
56B → ▲	6, 3.5, 4, 5	248	1.03	255
52A → ●	12, 7, 8, 8	145	1.8	261
52B → ■	12, 7, 16, 16	128	3.6	460

- RESULTS FROM 15-STAGE RING OSCILLATOR MEASUREMENTS
- WAFER NO. 7-2
- V_p = 0.95 V
- $\bar{\tau}_D$ AND $\bar{P}_D$ ARE THE AVERAGE OF THE FUNCTIONAL DEVICES
- SAMPLE SIZE EQUALS 44 DEVICES PER CIRCUIT

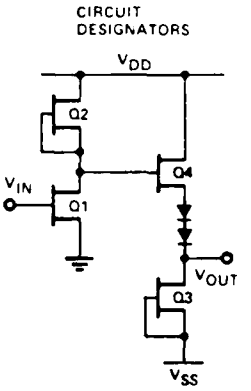

Fig. 3.1-12 GaAs gate array ring oscillator test results.

The predicted values of cell speed and cell power were 150 ps at 1.8 mW. The average measured value was 240 ps at 0.9 mW. The matching of the speed-power-product of the predicted value and measured results was quite good. However, the measured absolute value of the cell delay and cell power were different in value when compared to the predicted values. This difference can be attributed to two factors. First, the threshold voltage of the measured devices was lower than the calculated value, causing a reduction in the gate speed and power. Next, a comparison was done by comparing the average measured values to the simulated values. If only the fastest devices were included in the averaging, the difference between the measured and predicted results would decrease.

Loaded ring oscillators were also measured to determine the cell's speed performance as a function of loading. The ring oscillators were arranged in a 15-stage ring with each stage of the ring driving a known load capacitance. The load capacitance used during these tests consisted of interdigitated metal lines of both Schottky and second layer metal. These metal lines were arranged with a pitch and width which replicates the actual gate array metalization. The results of the testing, shown in Fig. 3.1-13, clearly show the expected linear degradation with loading. For the low drive cell configuration, the measured loading curve was 3.23 ps/FF, while the high drive cell configuration yielded a slope of 1.25 ps/FF. These numbers can be used to predict cell performance as a function of loading.

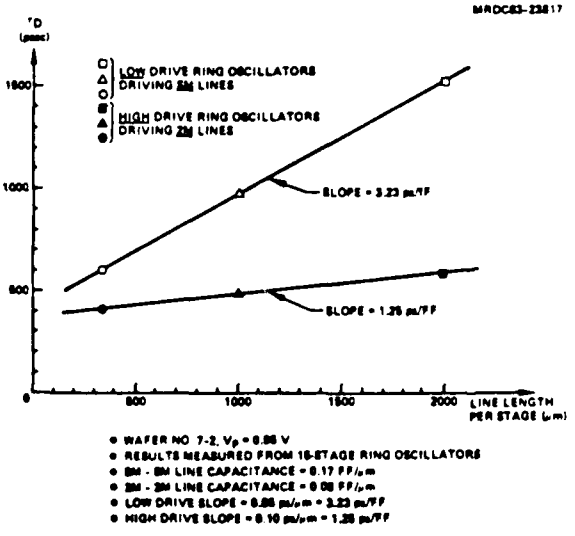

Fig. 3.1-13
GaAs gate array cell characterization test results.

3.1.6 5 x 5 Multiplier Test Results

The performance characterization of the 5 x 5 bit fixed precision multiplier test vehicle was carried out in two distinct steps. First, a low frequency functionality test was performed with the aid of a test stand employing a commercial minicomputer. Verification of the operation of the multiplier for 100% of the gates was obtained for several ICs; the best wafer yield achieved was 8%. Evaluation of high speed performance of the multiplier was facilitated by the use of an externally controllable on-chip feedback path. The feedback path, when enabled, routes the complement of the most significant output bit (P9) to the least significant input bit (A_0). The network of half and full adders comprising the multiplier was, in effect, converted into an asynchronous "oscillator". With the feedback path enabled and the input operand values of A = 10000 and B = 11111, an oscillator condition occurred. The half period of oscillation in this test is 15 τ_D. Measurement of the oscillation frequency allowed an inference of the average gate delay, τ_D. Figure 3.1-14 illustrates the oscillation waveform in the self-test oscillation mode. The oscillation frequency measured was 107 MHz, which corresponds to an average gate delay of 310 ps. With a worst case path delay of 21 τ_D for the multiplier, a 10 bit product could be achieved in 6.5 ns. The performance of several multipliers is summarized in Table 3.1-1.

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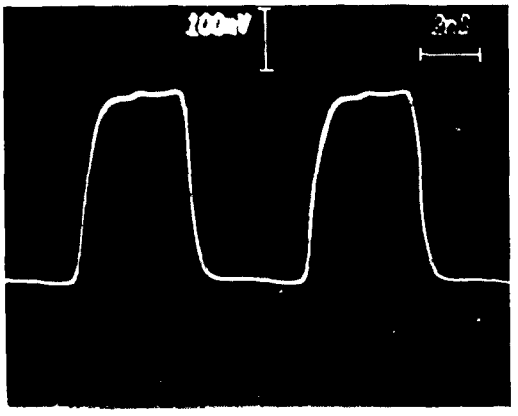

Fig. 3.1-14
Oscillation waveform in the self-test "oscillation" mode.

V_{DD} = 2.50V		F_{OSC} = 107.6 MHz	
V_{SS} = −1.50V		P_{sgate} = 2.79 mW	
T_d = 3.10 psec		$T_d \times P_d$ = 864	

Table 3.1-1

Performance Summary of the 5 x 5 Parallel Multiplier

Threshold Voltage (V_p)	Power Dissipation/Cell (P_D)	Propagation Delay/Cell (τ_D)	Speed/Power Product (τ_D) • (P_D)	Multiply Time
0.733	1.30 mW	740 ps	960 fJ	15.5 ns
0.890	1.97 mW	490 ps	960 fJ	10.3 ns
1.15	2.79 mW	310 ps	864 fJ	6.5 ns

To verify that the multiplier operated over a wide supply range, several fully functional multipliers were examined as a function of supply voltage. The two supply voltages, V_{DD} and V_{SS}, were varied and the multiplier operation was recorded. The BFL circuitry exhibited a high tolerance to supply variation, as shown in Fig. 3.1-15. Operation of the multiplier was obtained with V_{DD} ranging from 2.25 V to 3.0 V, and with V_{SS} ranging from -1.25 V to -2.0 V.

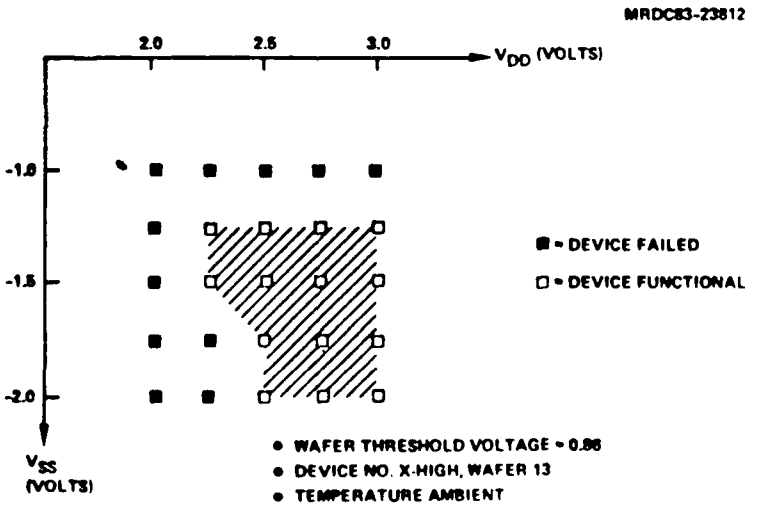

Fig. 3.1-15 GaAs gate array 5 x 5 multiplier test results working voltage range.

3.1.7 Gate Array Yield Data

The first yield test to be performed with the AR7 wafers was to correlate yield to V_{TH} variations, particularly at the edge of the wafer, and to make a preliminary comparison of 4X vs 10X projection lithography. The circuit which was utilized for these purposes was a small SDFL 7-stage ring oscillator which had been previously used as a standard for 1 inch processing. Two versions of the circuit were used; one with a 3 μm n^+ spacing for the FETs, and one with a 2.5 μm n^+ spacing. The tests confirmed that the majority of circuit failures were at the edge of the wafer. Dielectric deposition techniques, etching non-uniformities and wafer handling all contribute to the observed edge effects. For both versions of the circuit, the yield for the center 32 fields was 94%, while the yield for all 44 fields was 82%. Since the yield for both versions was the same, the tighter design rules for the 10X lithography system do not appear to be a problem. This is in contrast to the 4X system in which a notable decrease in circuit yield (≈ 70%) was noted for the smaller n^+ gap.

The majority of the AR7 mask set was devoted to gate array circuits, of which three types were used for a preliminary yield evaluation. These circuits included 15-stage ring oscillators, 15-stage ring oscillators driving metal lines and crossovers and, finally, 5 x 5 multipliers. The chip size varied from 0.37 mm^2 for the small ring oscillators to 5.2 mm^2 for the 5 x 5 multiplier. Yield data was collected at the time of circuit testing (Sec. 3.0) from five wafers. The results can be presented in two ways; yield as a function of chip size, and secondly, yield as a function of gate count. Yield data for the AR7 circuits are shown in Figs. 3.1-16 and 3.1-17, along with data from SDFL custom designs on 1 inch wafers. The data for the 3 in. wafers are presented, both including and excluding the 12 edge fields of the wafer. From the yield vs area plot, it is possible to determine a random defect density of 60 defects/cm^2 for the gate array wafers. Visual inspection of the wafers show fairly large defects of the type shown in Fig. 3.1-18, where photoresist defects and equipment-related deposits appear to be a major contributor to the defect density.

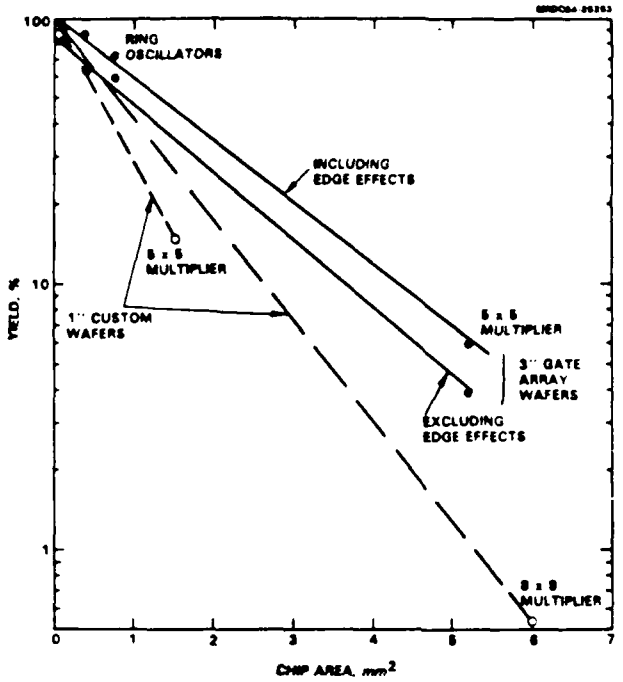

Fig. 3.1-16
Yield data for gate array and custom circuits based on chip area.

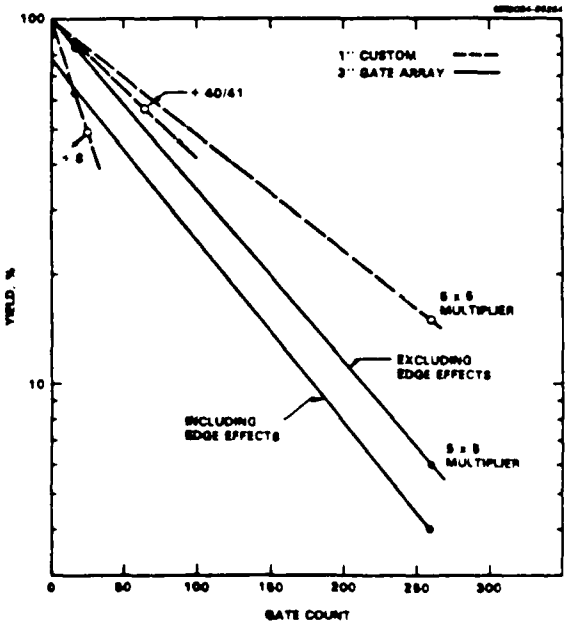

Fig. 3.1-17
Yield data for gate array and custom circuits based on gate count.

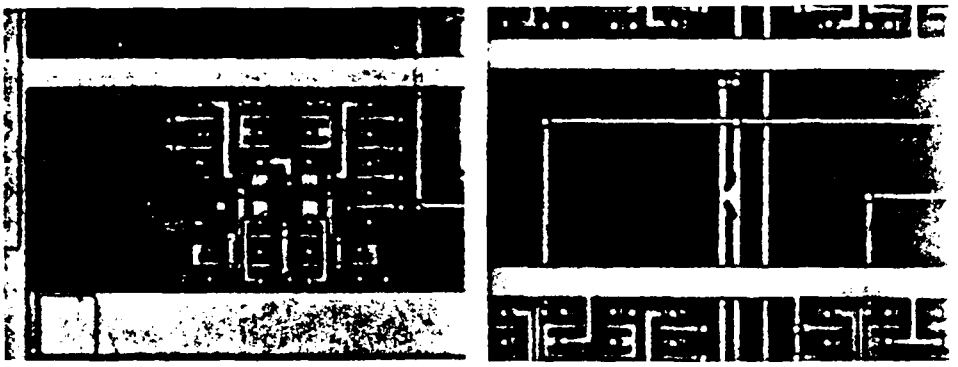

Fig. 3.1-18 Examples of AR7 wafer defects.

When comparing the custom 5 x 5 multiplier to the gate array multipliers, a number of observations can be made. The yield of the custom design is higher than that of the gate array design based on gate count; however, the gate array chip is 3.7 times larger. Thus, when considering equal area chips, the gate array designs have higher yield. Another factor which influences yield for the two designs is packing density. The gate array design, which has 90% utilization, is less dense than the custom design. On the other hand, the gate array utilizes longer lengths of second level interconnect metal which is shown to be a primary yield limiting factor. In summary, a direct comparison of the custom and gate array multipliers is difficult to make in terms of yield limits.

3.2 AR8 Mask Set

The AR8 mask set was the second phase of the GaAs gate array development. It contained an array of 1K equivalent uncommitted BFL gates in the medium speed/power range of the technology. It is an expansion of the AR7 gate array and uses the same basic cell design. The objective of this iteration is to demonstrate the capability of a large array of uncommitted logic that can be customized for rapid design turnaround. The computerized auto placer and router developed by Mayo Foundation was used to customize two arrays. Test cells were included to monitor the process, to characterize the arrays, and to evaluate the performance of the circuits. In addition, some operational amplifier circuits developed at University of California, Santa Barbara were included on the mask set.

3.2.1 AR8 Reticle Layout

The reticle layout consisted of the 1K gate arrays each of which occupied approximately one quarter of the available reticle area. Two of the arrays were customized by the computer program developed at Mayo. The two circuits were an eight-bit parallel multiplier and a portion of the protocol circuit of the AOSP bus, respectively. The third array was a test array to characterize library macro-cells in a real environment. The major macros used in the multiplier and AOSP circuits were isolated, and connected to appropriate I/O. Four shift register test circuits were designed for evaluation along with a signal cross-coupling test circuit. All of these circuits were built on the actual 1K gate array floor plan. The fourth quandrant was a pattern of test circuits. Individual patterns of the basic cell, I/O cell, FETs, and resistors were built for evaluation of the components. A ring oscillator was duplicated from AR7 for comparison of speed. The 5 × 5 multiplier was also duplicated from AR7 so that yield comparisons could be made. A layout of the AR8 reticle is shown in Fig. 3.2-1.

3.2.2 AR8 Test Results

The preliminary testing of the AR8 mask set was divided into two parts. The initial investigation concentrated on test structure evaluation transfer function analysis, and ring oscillator performance. The final testing concentrated on 5 × 5 and 8 × 8 multiplier functionality. Because of time limitations, and mask error corrections, only three standard processed wafers were made available for testing during this time. Thus, the results are not as completed as would normally be desired, since data from several runs are usually necessary to obtain complete functionality information.

Of the 15 various test cells lifted from the actual 1K array, only a few were tested since portions of the actual array were found to be functional. Of primary interest was the analysis of the inverter transfer function over the mil-spec temperature range. As seen in Fig. 3.2-2, the output swing was reduced as the temperature was lowered from 25°C to -55°C. Th opposite was true for increased temperature operation up to 125°C. High temperature operation also

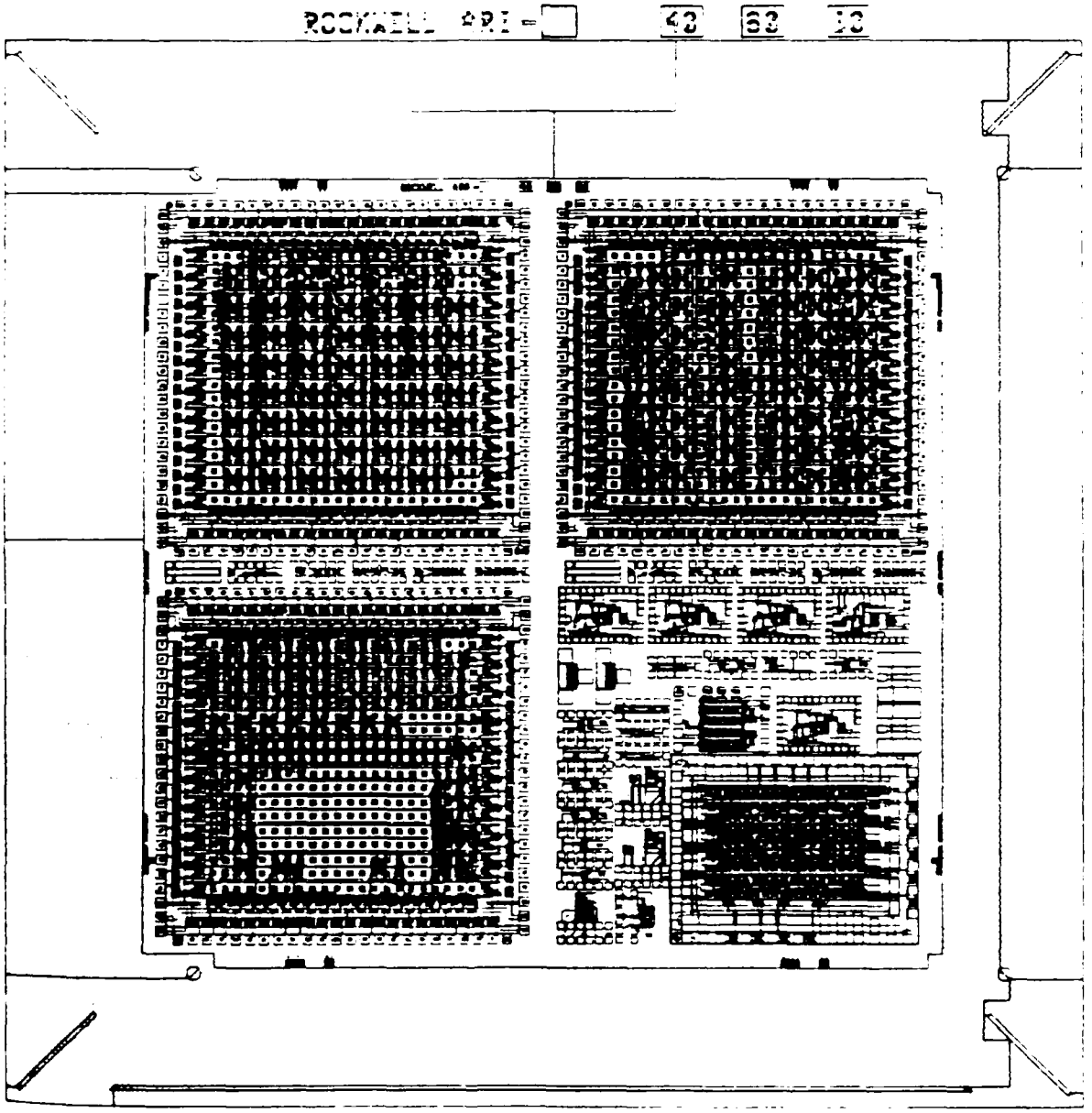

Fig. 3.2-1 AR8 mask set layout.

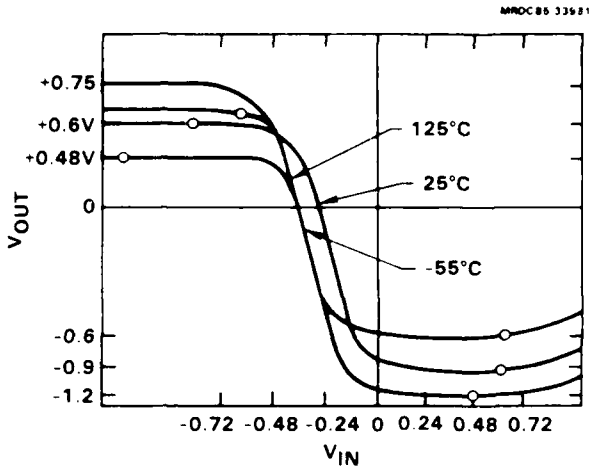

Fig. 3.2-2 Transfer characteristics as a function of temperature.

caused a slight reduction in low level noise margin as evidenced by the approximate 120 mV shift in the unity gain point. Variations in the transfer characteristics with respect to the negative supply voltage, V_{SS}, were also measured at room temperature (Fig. 3.2-3). As expected, the output low level was the point most significantly effected, usually being 250 mV more negative as V_{SS} was varied from -1.0 V to -2.0 V.

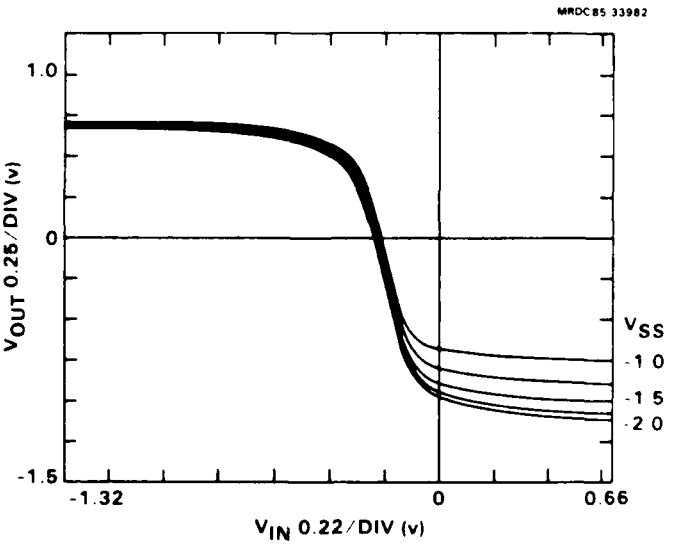

Fig. 3.2-3
Transfer curves as a function of V_{SS}.

Ring oscillators lifted from the previous gate array mask set (AR7) were also tested. This circuit consisted of two 15-stage ring oscillators, laid out using standard gate array cells; with one oscillator using cells configured for high output drive capability, and the other using cells configured for lower output drive capability, commensurate with reduced power consumption. These oscillators were tested on two wafers with the results tabulated below.

Delay (pS)			(Volts)		
Avg.	Fastest	Slowest	V_{dd}	V_{ss}	V_{bb}
162	137	222	2.5	1.6	2.5
162	131	333			
136	114	165	2.5	1.7	2.5
146	121	198			

The speed power products are not available because both oscillators were biased simultaneously, using the same power supplies. However, since the differences between the two ring oscillators is not dramatic, and most gate arrays will have a combination of high power and low power gates, the average power dissipations and speed power products are as follows:

V_{dd}	I_{dd}	V_{ss}	I_{ss}	V_{bb}	I_{bb}	Avg. Pd (mW)	Avg. Pt (fJ)
2.5	23	1.6	18	2.5	10	2.88	429
2.5	26	1.7	20	2.5	10.6	3.29	463

V = volts

I = milliamps

These results are consistent with the ring oscillator tests performed using the AR7 mask set.

The final test device to be probed was the full adder circuit. This circuit was found operational over a wide operating range with a yield of approximately 80%. A plot showing the operating range of the adder is shown in Fig. 3.2-4.

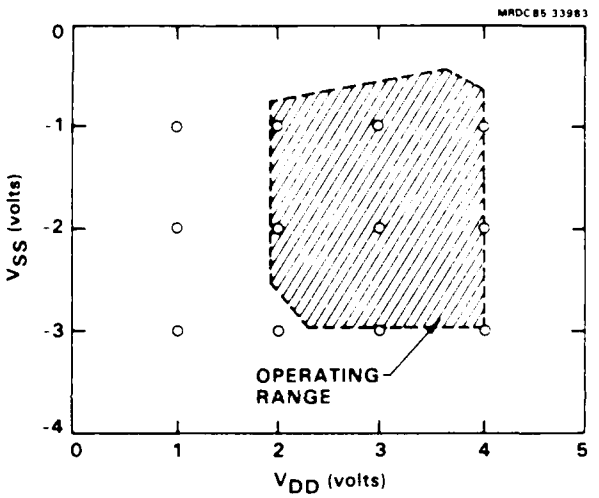

Fig. 3.2-4 Room temperature operating range of full adder.

The 5 × 5 multiplier circuit, also lifted from the AR7 mask set, was the next circuit to be tested. The yield was approximately 1% as compared to approximately 5% on the previous wafers. The major sympton of failure was a very small output swing (on the order of several tens of millivolts). Power supply levels and operating performance of the multiplier was consistent with previous operation.

In addition to the 5 × 5 multiplier, the 8 × 8 multiplier was also tested during this time. This circuit was the first to be fully auto-routed by the Mayo Foundation utilizing their recently developed software.

This circuit was tested using an H.P. 8180 word generator, and an H.P. 8182 data acquistion unit. No fully functional parts were found, due to a mask defect (incomplete chromium removal) in one of the full adder sections, which caused a repeatable error, observable in the P2 output. A simple set of test

vectors was used to detect the defect. Shown below is a portion of the test vectors used, along with the expected output data, and a sample of the typical output data observed.

	Multiplier Input Words		Multiplier Output Words (Expected)	(Typical)
	AAAAAAAA	BBBBBBBB	PPPPPPPPPPPPPPPP	PPPPPPPPPPPPPPPP
			1111111111111111	1111111111111111
	76543210	76543210	5432109876543210	5432109876543210
0	11111111	11111111	1111111000000001	1111110011100001
1	00000001	11111111	0000000011111111	0000010011001011
2	11111111	00000001	0000000011111111	0000000011111111
3	00000001	00000001	0000000000000001	0000000000000101
4	00000010	00000001	0000000000000010	0000000000000110
5	00000100	00000001	0000000000000100	0000000000001100
6	00001000	00000001	0000000000001000	0000000000010100
7	00010000	00000001	0000000000010000	0000000000100100
8	00100000	00000001	0000000000100000	0000000001000100
9	01000000	00000001	0000000001000000	0000000010000100
10	10000000	00000001	0000000010000000	0000000100000100
11	00000000	00000000	0000000000000000	0000000000000000

The error that was detected would have made any test done with vectors utilizing the feedback loop meaningless, so they were not performed. The fact that the output states were not completely consistent for even the simple test pattern indicates that there is a yield problem, in addition to the mask defect problem.

Again, the major difficulty in obtaining good multiplier results centered on the limited number of "good" wafers. However, the auto-routing techniques and preliminary test results indicate a reasonable start to large area gate array fabrication.

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